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Online Calibration of a Nyquist-Rate Analog-to-Digital Converter Using Output Code-Density Histograms

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***Abstract*—A scheme for the online correction of static nonlinearities in a Nyquist-rate analog-to-digital converter (ADC), using output code-density histograms, is presented. The estimation of the integral nonlinearity (INL) at each output level, followed by the creation of a corresponding entry in the look-up table for error correction, is analytically explained. The suitability of the scheme for calibrating high-end ADCs has been demonstrated. An extra ADC and the associated switching and postprocessing DSP circuitry along with some memory for storing the data to be processed, are the overhead in this scheme. An improvement of over 20 dB in the spurious-free dynamic range, from an uncalibrated value of over 80 dB, has been achieved.**

***Index Terms*—Analog-to-digital converter (ADC), code density, online calibration, static nonlinearity.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are the backbone of mixed-signal systems. With increasing performance requirements on ADCs, the limitations of IC fabrication technologies in providing adequately low levels of signal distortion are becoming more and more apparent. Calibrations are routinely performed on high-performance ADCs to ensure the degree of accuracy they are designed for and to withstand aging of system components. However, with increasing complexity of ADCs and, consequently, increasing time and cost of periodic testing and calibration, self-calibrating systems capable of online nonlinearity correction are gaining attention. A scheme for the implementation of such a self-calibrating ADC system, automatically correcting its static nonlinearities while it continuously processes real-time input signals, is the subject of this paper.

The organization of this paper is as follows. Section II presents the background elements and the definition of the problem to be solved. The basic idea behind the calibration scheme as well as the most important bottle-necks to be overcome are presented in Section III. The detailed analysis of the procedure followed for calibration is explained in Section IV. Circuit overhead is estimated in Section V. Simulation results are presented in Section VI, followed by the conclusion in Section VII.

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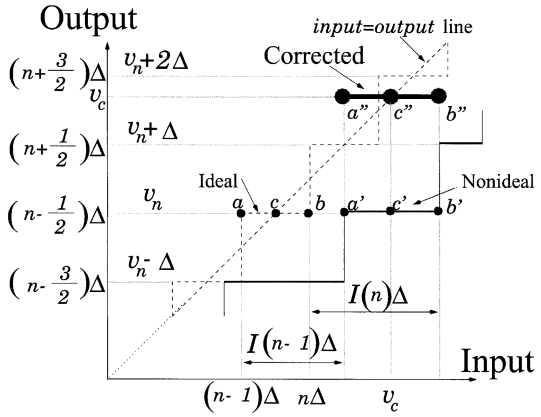

Fig. 1. Illustration of the best possible correction.

II. Background

Let us consider a q-bit ADC with input dynamic range from $-F/2$ to $F/2$. Its ideal step size Δ is given by $\Delta = F/(N-1)$, where $N = 2^q$ is the total number of output levels. Ideally, the probability density function (PDF) of the quantization error is uniform inside the interval $[-\Delta/2, \Delta/2]$ at a value of $1/\Delta$ and is zero outside it. Let an output level or bin v_n be represented by n, such that $v_n = [n-1/2]\,\Delta$. The full set of available values for n is given by $B = \{-N/2+1, -N/2+2, \ldots, -1, 0, 1, \ldots, N/2\}$.

A. Correction Based on Estimated INL

An ADC's static nonlinearities are completely described by its static input versus output characteristics. Fig. 1 shows the ideal as well as a typical nonideal static characteristic, while also illustrating the *best possible* correction. The line segments $\overline{ab}$, $\overline{a'b'}$, and $\overline{a''b''}$, respectively, represent the ideal, nonideal, and corrected locations of output level n. v_c is the average input amplitude that corresponds to the nonideal location of n. It is then obvious that the best possible correction is achieved by shifting the output level n to the value of its average input, i.e., v_c. The value of the shift, given by the length of the line segment $\overline{c'c''}$, is also given by the length of line segment $\overline{cc'}$, since $cc'c''$ is an isosceles right-angeled triangle. Moreover, since c and c' are the mid-points respectively of line segments $\overline{ab}$ and $\overline{a'b'}$, $cc' = (aa' + bb')/2 = [I(n-1) + I(n)]\,\Delta/2$, where $I(n-1)$

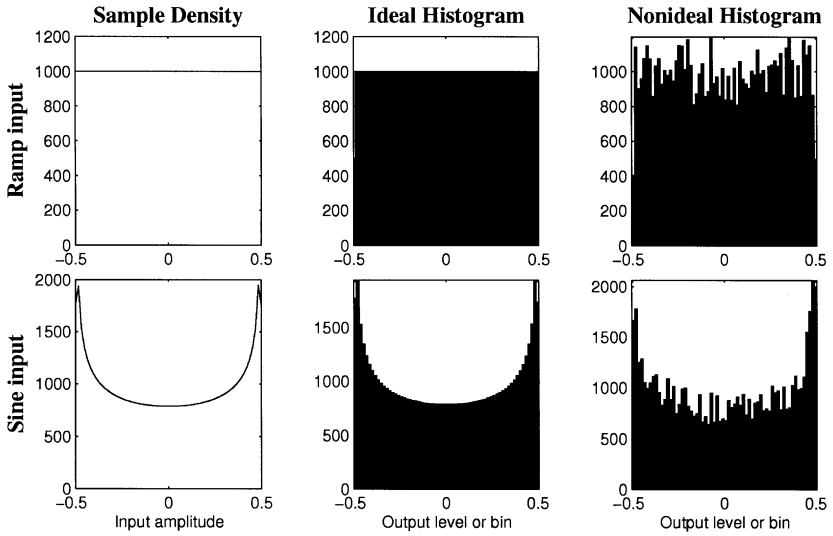

Fig. 2. Ideal and nonideal output histograms for a slow ramp and sinusoidal inputs.

and $I(n)$ represent the integral nonlinearity (INL) in least-significant-bit (LSB) units, at output levels $(n-1)$ and n, respectively. (Note: offset and gain errors have been included in INL.) Hence

$$v_c = v_n + \left[\frac{I(n-1)+I(n)}{2}\right]\Delta = \left[n + \frac{I(n-1)+I(n)-1}{2}\right]\Delta. \quad (1)$$

Determination of INL at each output level enables such a correction for all the possible outputs.

B. Offline Calibration Versus Online Calibration

The use of output code density test methods to estimate INL and correct for it has been well established over the years. Offline calibration methods derive the INL by using specific test signals (known *a priori*), like a slow ramp or a full-scale sine wave [1]–[7]. A large number of samples are collected, and the output code density is plotted as a histogram. The nonidealities are estimated by comparing the histogram thus obtained, with a reference histogram that corresponds to an ideal ADC, as shown in Fig. 2.

Offline calibration methods, however, suffer from the following drawbacks.

1) The generation of sufficiently precise input *analog* test signal becomes more and more difficult with increasing ADC resolution and quality of calibration. Existing on-chip implementations of such signal generators are unreliable, needing expensive off-chip signal generators and testers.
2) Offline calibration requires the ADC to be taken offline for calibration regularly enough to compensate for aging errors, etc., needing expensive test-time budgets as well as possibly leading to interruptions in data conversion which may not be tolerable in some applications.

In order to counter long interruptions, several methods for background calibration were proposed. Traditional correction techniques can be used if a time-slot for background calibration is made available. The skip-and-fill algorithm [8] enables an occasional calibration time-slot: the input sample is skipped and is replaced by a calibration signal. Then the missing output is filled in through polynomial interpolation. Another approach uses a queue-based architecture [9] for creating calibration time-slots. However, since these methods require a calibration signal, the overall accuracy depends on the one of the calibration signal. Moreover, the calibration applies to only a section of the converter (like a cell of a pipeline architecture) and normally does not include the input sample and hold (S/H). Other schemes, like the one proposed in [10], require the addition of calibration signals to the input, thus limiting the usable dynamic range of the data converter. These methods of background calibration are not truly online and depend heavily on the generation of precise analog signals.

The drawbacks of offline and background calibrations mentioned above are countered well by resorting to online calibration, which exhibits the following features [11], [12].

1) The ADC is online always; its input is, hence, the real-time input, eliminating the need for the generation of precise analog test signals.
2) There is no time lost in testing nor is the data-conversion process interrupted from time to time for calibration.

C. Relation Between Code-Density Histogram, Amplitude Distribution, and DNL

For online calibration, however, since no known test signals are used, it is necessary to develop a scheme for a generic input signal with an unknown probability distribution of amplitude ρ. $\rho(v)$ represents the sample density at input amplitude v. Then, from Fig. 1, for a large number of samples on output level n, the output code-density function or histogram H is given as

$$H(n) = \int_{[n-1+I(n-1)]\Delta}^{[n+I(n)]\Delta} \rho(v)dv \approx \rho(v_c)[1+I(n)-I(n-1)]\Delta \quad (2)$$

assuming linear variation of ρ within the small interval $[[n-1+I(n-1)]\Delta, [n+I(n)]\Delta]$, and with v_c given by

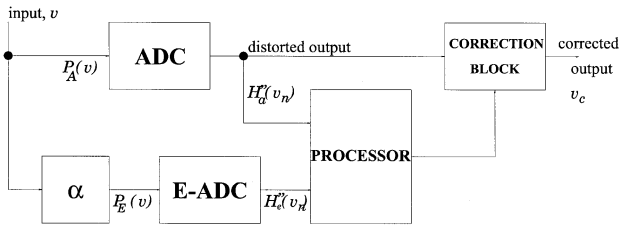

Fig. 3. Schematic representation of the proposed self-calibrating ADC system with online error correction.

(1). Defining the normalized amplitude-distribution function (NADF) P as

$$P(v) = \rho(v)\Delta \tag{3}$$

(2) reduces to

$$H(n) = P(v_c)\,[1 + D(n)] \tag{4}$$

where $D(n)$ represents the differential nonlinearity (DNL), in LSB units, at n, related to INL by definition as

$$D(n) = I(n) - I(n-1). \tag{5}$$

The aim is to solve for INL from (4) and (5), using the known value of INL at some output level as the starting point.

III. Calibration Scheme

Offline calibration methods rely on the prior knowledge of the input signal's NADF P, causing (4) to be easily solved by simply constructing the output histogram. In the case of online calibration, however, P is unknown. Hence, more information than a single output histogram needs to be generated.

The proposed self-calibrating ADC system is schematically shown in Fig. 3. Two independent measurements are made on each input sample—one using the ADC to be calibrated, referred to as ADC, and the other using an extra ADC (E-ADC). E-ADC measures the input sample after it is attenuated by a factor α. ADC and E-ADC are both real ADCs exhibiting monotonicity and with no missing codes.

Even before getting into a detailed analysis of this scheme, the following conclusions can be drawn.

1) The signal path through E-ADC provides the additional data required to overcome the unknown nature of the input signal's NADF, P.
2) The resolution of calibration is directly influenced by the resolution of E-ADC—the higher the resolution of E-ADC, the better the calibration. However, in practice, the highest resolution of E-ADC is that of ADC.
3) The introduction of additional analog/mixed-signal blocks (like attenuator and E-ADC) prone to component variations, however, further increases the number of unknown quantities in the self-calibrating system which are manifested as the *uncertainty* in the actual value of α and the *mismatch* between ADC and E-ADC.

Section IV explains in detail the theory and procedure of the calibration scheme for the case when ADC and E-ADC have the same nominal resolution and dynamic range. Emphasis is laid on the techniques used to overcome the practical limitations and bottle-necks created by the introduction of additional analog/mixed-signal blocks.

IV. Calibration Theory and Procedure

A large number of samples are collected at the outputs of ADC and E-ADC, and their output histograms, H_a'' and H_e'', respectively, constructed. The input NADFs of ADC and E-ADC, P_A and P_E, respectively, then follow

$$\alpha P_E(\alpha v) = P_A(v). \tag{6}$$

Further, from (4), we have

$$\begin{aligned} H_a''(n) &= P_A(v_{c,a})\,[1 + D_a(n)] \\ H_e''(n) &= P_E(v_{c,e})\,[1 + D_e(n)] \end{aligned} \tag{7}$$

where D_a and D_e are respectively the DNLs of ADC and E-ADC, and, from (1), since ADC and E-ADC have the same ideal step-size Δ

$$\begin{aligned} v_{c,a} &= v_n + \left[\frac{I_a(n-1) + I_a(n)}{2}\right]\Delta \\ v_{c,e} &= v_n + \left[\frac{I_e(n-1) + I_e(n)}{2}\right]\Delta \end{aligned} \tag{8}$$

where I_a and I_e are, respectively, the INLs of ADC and E-ADC.

Without knowing the relationship between I_a and I_e, the INL of ADC cannot be determined using (6)–(8). Moreover, the actual value of α has some uncertainty added to its designed (desired) value. The procedure involving overcoming these bottlenecks on the way to determining the INL of ADC is summarized in the following three conceptual steps:

1) preconditioning the output histograms to effectively eliminate the mismatch between ADC and E-ADC (Section IV-A);
2) estimation of ADC's offset and the *actual* value of α (Section IV-B);
3) determination of INL after reduction to the case when E-ADC is effectively matched with ADC (Section IV-C), followed by the creation of a look-up table (LUT) for correction.

A. Preconditioning the Histograms—Mismatch Elimination

ADC and E-ADC are affected by different static nonidealities (offset, gain, and INL/DNL errors), leading to an unknown amount of mismatch between them. Knowledge of this mismatch is a prerequisite for calibration using the proposed scheme.

The mismatch information is obtained by changing the value of α in Fig. 3 to unity. This phase with $\alpha = 1$ will be referred to as the mismatch-estimation phase during which, as before, a large number of samples are collected at the outputs of ADC and E-ADC and their output histograms, H_a^* and H_e^*, respectively, are constructed.

Let us consider the input interval $\boldsymbol{V}_a = [V_{a,\min}, V_{a,\max}]$ that determines the domain of all samples that hit the output level a of ADC. Since both the ADCs are monotonic, the input samples from the same interval $\boldsymbol{V}_a$ cause hits on a set of *consecutive* output levels on E-ADC. Let the first of these consecutive output levels on E-ADC, for a given output level a on ADC, be denoted by e_a. There are three different possibilities (see Fig. 4):

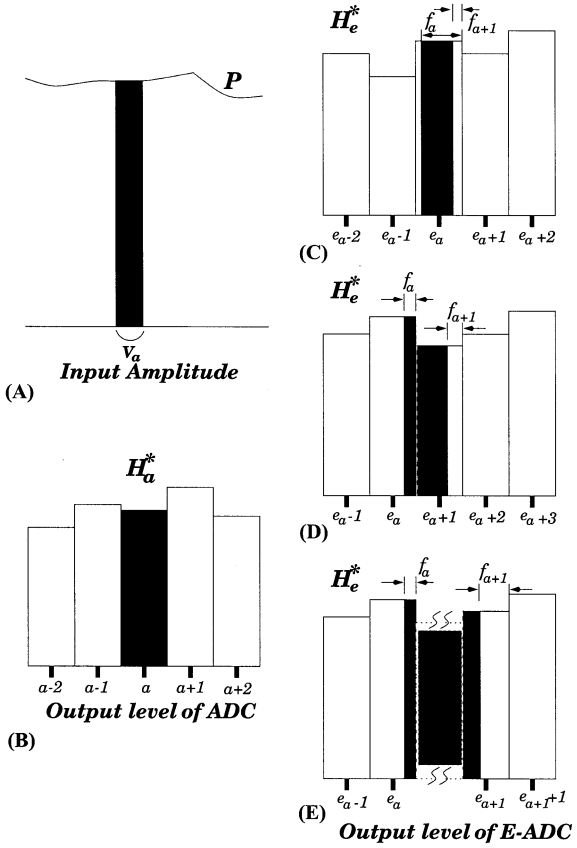

Fig. 4. Mapping representing the mismatch. (a) Input NADF, P, with the interval $V_a = [V_{a,\min}, V_{a,\max}]$ shaded. (b) Histogram of ADC with output level a shaded. (c) Shaded region on the histogram of E-ADC corresponding to output level a on ADC for the case when $e_{a+1} = e_a$. (d) Corresponding shaded region on the histogram of E-ADC for the case when $e_{a+1} = e_a + 1$. (e) Corresponding shaded region on the histogram of E-ADC for the case when $e_{a+1} > e_a + 1$.

1) $e_{a+1} = e_a$: output bin a of ADC is mapped completely *into* one output bin e_a of E-ADC;
2) $e_{a+1} = e_a + 1$: output bin a of ADC is mapped completely into two adjacent output bins e_a and $e_a + 1$ of E-ADC;
3) $e_{a+1} > e_a + 1$: output bin a of ADC is mapped completely into more than two consecutive output bins $\{e_a, e_a + 1, \ldots, e_{a+1}\}$ of E-ADC.

In Fig. 4, let f_a represent the fraction of the e_ath bin from the beginning of shading to the end of the bin. The task of the mismatch-estimation phase is to determine the values of output level e_a on E-ADC and the corresponding fraction f_a for each output level a on ADC. This information is sufficient to completely characterize the mismatch between ADC and E-ADC.

To determine these values, accumulated histogram functions S_a^* and S_e^*, defined as in (9) for any bins a on ADC and e on E-ADC, are constructed as follows:

$$S_a^*(a) \equiv \sum_{n=-(N/2)+1}^{a-1} H_a^*(n)$$
$$S_e^*(e) \equiv \sum_{n=-(N/2)+1}^{e-1} H_e^*(n). \tag{9}$$

Then, for each output level a of ADC

$$S_e^*(e_a) \le S_a^*(a) < S_e^*(e_a + 1) \tag{10}$$

from which the value of e_a can be computed. The corresponding fraction f_a is given by

$$f_a = \frac{S_e^*(e_a + 1) - S_a^*(a)}{H_e^*(e_a)}. \tag{11}$$

The information required to precondition the original histograms H_a'' and H_e'' [defined in (7)] is now available. This preconditioning is done in order to mimic the case when E-ADC is matched with ADC. The process of preconditioning involves constructing two new histograms, H_a' and H_e', such that

$$\begin{aligned} H_e'(a) &\equiv [f_a - f_{a+1}]\, H_e''(e_a), \quad e_a = e_{a+1} \\ &\equiv f_a H_e''(e_a) + [1 - f_{a+1}]\, H_e''(e_{a+1}), \\ e_{a+1} &= e_a + 1 \\ &\equiv f_a H_e''(e_a) + [1 - f_{a+1}]\, H_e''(e_{a+1}) \\ &\quad + \sum_{n=e_a+1}^{e_{a+1}-1} H_e''(n), \quad e_{a+1} > e_a + 1 \end{aligned}$$

and

$$H_a'(a) \equiv H_a''(a). \tag{12}$$

Note that, actually, only one new histogram is constructed; the histogram of ADC undergoes no pre-conditioning. However, for the sake of consistency in notation, H_a' is used instead of H_a''. Effectively, it can be stated that, if E-ADC were actually matched with ADC, we would have obtained H_a' and H_e' as the original output histograms instead of H_a'' and H_e''.

After pre-conditioning to eliminate mismatch, effectively

$$I_e = I_a = I \tag{13}$$

and

$$D_e = D_a = D \tag{14}$$

reducing (7) and (8) to

$$\begin{aligned} H_a'(n) &= P_A(v_c)\,[1 + D(n)] \\ H_e'(n) &= P_E(v_c)\,[1 + D(n)] \end{aligned} \tag{15}$$

with v_c given by (1).

B. Estimation of ADC's Offset and the Actual Value of α

Once the mismatch between ADC and E-ADC is removed, the accuracy of calibration is influenced by the linearity of the attenuator—the higher the attenuator linearity is, the better the calibration. In practice, the need is for an attenuator whose linearity is better than the desired linearity (after calibration) of the self-calibrating ADC system. A simple implementation of a highly linear attenuator is by using a resistive divider with $\alpha = 0.5$. For this value of α, the voltage and temperature coefficients of the identical resistors used in the divider effectively cancel each other, keeping the divider very linear throughout the dynamic range of operation.

Accurate estimation of the static errors in ADC requires a precise knowledge of the value of α. However, the design of a precise analog gain stage is difficult. Hence, it is imperative to

estimate the actual value of α (which invariably differs from its designed value of 0.5) to a high degree of accuracy. Substituting $v = 0$ in (6) and using (15) gives

$$\alpha = \frac{P_A(0)}{P_E(0)} \approx \frac{H'_a(n_{\text{off}})}{H'_e(n_{\text{off}})} \tag{16}$$

where n_{off} is the output level on to which the offset of ADC V_{offset} (defined as the output value for zero input) is coded such that $[n_{\text{off}} - 1]\,\Delta \leq V_{\text{offset}} < n_{\text{off}}\Delta$. The approximation is because of the discrete nature of the argument of the histograms. A more accurate version of (16) is

$$\alpha = \frac{H'_A(V_{\text{offset}})}{H'_E(V_{\text{offset}})} \tag{17}$$

where H'_A and H'_E are the interpolated versions of H'_a and H'_e, respectively. Hence, the offset value of ADC is needed to estimate the actual value of α.

1) Estimation of the Offset Error: To estimate the offset error, we will use a beautiful property [shown in (19)] exhibited by the accumulated histograms S'_a and S'_e defined as

$$\begin{aligned} S'_a(a) &\equiv \sum_{n=-(N/2)+1}^{a-1} H'_a(n) \\ S'_e(e) &\equiv \sum_{n=-(N/2)+1}^{e-1} H'_e(n). \end{aligned} \tag{18}$$

Irrespective of the value of α, if ADC and E-ADC are matched and of *infinite* resolution, then

$$S'_a(n_{\text{off}}) = S'_e(n_{\text{off}}) = \int_{-\infty}^{0} P_A(v)dv = \int_{-\infty}^{0} P_E(v)dv. \tag{19}$$

Defining

$$\delta S'(l) \equiv S'_a(l) - S'_e(l) \tag{20}$$

where l is any output level, it can be easily seen that, if the resolution of the *matched* ADCs is *infinite*, $\delta S'$ passes through zero at n_{off} as shown in Fig. 5. However, in the case of *finite* resolution ADCs, a change of sign is observed between $\delta S'(n_{\text{off}})$ and $\delta S'(n_{\text{off}} + 1)$. In particular, for $\alpha < 1$

$$\delta S(n'_{\text{off}}) \geq 0, \quad \delta S'(n_{\text{off}} + 1) \leq 0. \tag{21}$$

Assuming linear variation of $\delta S'$ around n_{off}, the offset value of ADC is computed as

$$V_{\text{offset}} = \left[n_{\text{off}} - 1 + \frac{|\delta S'(n_{\text{off}})|}{|\delta S'(n_{\text{off}})| + |\delta S'(n_{\text{off}} + 1)|} \right] \Delta. \tag{22}$$

2) Elimination of the Contribution of Offset to INL: Until now, INL has been treated as the total error at each output level. This included not only the static nonlinearities, but also the offset error. (It can be shown that the this scheme cannot detect gain error.) If the amplitude axis of the preconditioned histograms is shifted to V_{offset} to create new histograms H_a and H_e such that

$$\begin{aligned} H_A(v) &\equiv H'_A\left(v + V_{\text{offset}}\right) \\ H_E(v) &\equiv H'_E\left(v + V_{\text{offset}}\right) \end{aligned} \tag{23}$$

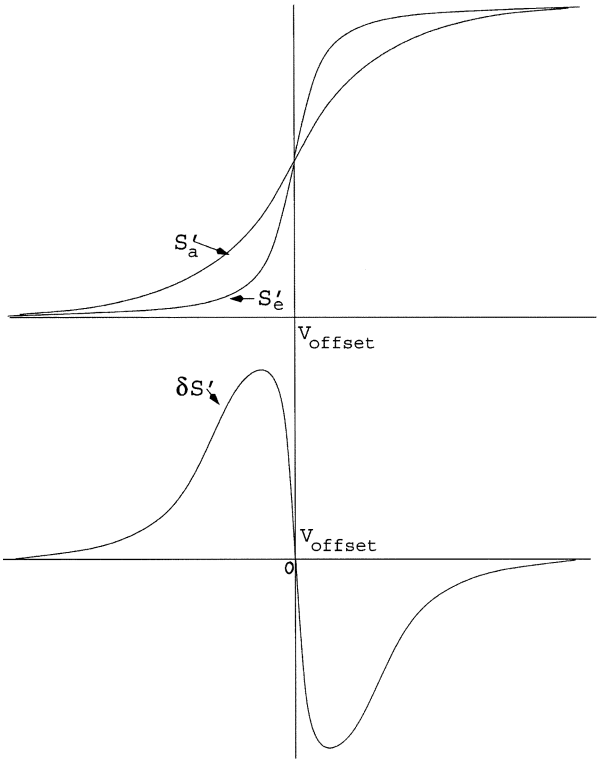

Fig. 5. The accumulated histograms S'_a and S'_e and their difference $\delta S'$.

where the relationships between H_a and H_e and their interpolated versions H_A and H_E are given by

$$\begin{aligned} H_a(n) &= H_A\left(\left[n - \frac{1}{2}\right]\Delta\right) \\ H_a(n) &= H_E\left(\left[n - \frac{1}{2}\right]\Delta\right). \end{aligned} \tag{24}$$

Effectively, under the new coordinates, the histograms mimic the case when the offset error is zero. With the offset error removed from the total error, INL can now be estimated starting with

$$I(0) = 0. \tag{25}$$

3) Accurate Value of α: Equations (17) and (23) together give

$$\alpha = \frac{H_A(0)}{H_E(0)}. \tag{26}$$

However, random local (within each output level) variations of the input NADF can lead to inaccurate calculations of α. A better evaluation is then provided by averaging out these local variations. Thus, for higher accuracy we have

$$\alpha = \frac{\sum_{p=1}^{M} \left\{ H_a\left([2p-1]\frac{\Delta}{2}\right) + H_a\left(-[2p-1]\frac{\Delta}{2}\right) \right\}}{\sum_{p=1}^{M} \left\{ H_e\left([2p-1]\frac{\Delta}{2}\right) + H_e\left(-[2p-1]\frac{\Delta}{2}\right) \right\}} \tag{27}$$

where M is a positive integer. M should be chosen large enough for sufficient averaging, but not too large since there is a possibility of the value of α then being corrupted by nonrandom trends in the variation of input NADF.

C. Solving After Reduction to the Task of INL Estimation Using Matched ADCs With Zero Offset

Defining $I'(x) \equiv I(x/\Delta)\,\Delta$, with I assumed to be linearly interpolated between the values n for which it has been originally defined, it can be shown that

$$I'(v_n) = \left[\frac{I(n-1)+I(n)}{2}\right]\Delta \tag{28}$$

which, from (1) represents the correction required on output level n. Defining a basis function g as

$$g(v) \equiv \frac{H_E(v)}{H_A(v)} \tag{29}$$

and using (1), (6), (15), and (28) yields

$$g(v_n) = \frac{H_e(n)}{H_a(n)} = \frac{P_E(v_c)}{P_A(v_c)} = \frac{P_E(v_n + I'(v_n))}{\alpha P_E(\alpha[v_n + I'(v_n)])}. \tag{30}$$

Replacing v_n in (30) by $v_n - I'(v_n)$ and assuming $|I'(v_n - I'(v_n)) - I'(v_n)| \ll |v_n|$ yields

$$\alpha g(v_n - I'(v_n)) \approx \frac{P_E(v_n)}{P_E(\alpha v_n)}. \tag{31}$$

It can be shown that

$$\begin{aligned} P_E(v_n) &= k \lim_{r\to\infty} \prod_{p=0}^{r} \alpha g\left(\alpha^p v_n - I'(\alpha^p v_n)\right) \\ P_A(v_n) &= \alpha k \lim_{r\to\infty} \prod_{p=1}^{r} \alpha g\left(\alpha^p v_n - I'(\alpha^p v_n)\right) \end{aligned} \tag{32}$$

where k is a scale factor, given by using (26) or (27) and (32), as

$$\begin{aligned} \alpha k &= H_A(0) \\ &\quad \sum_{p=1}^{M} \left\{H_a\left([2p-1]\tfrac{\Delta}{2}\right) + H_a\left(-[2p-1]\tfrac{\Delta}{2}\right)\right\} \\ &= \frac{}{2M}. \end{aligned} \tag{33}$$

From (15) and (32) we have

$$1 + D(n) = \frac{H_a(n)}{\alpha k} \lim_{r\to\infty} \prod_{p=1}^{r} \frac{1}{\alpha g\left(\alpha^p v_c - I'(\alpha^p v_c)\right)}. \tag{34}$$

Using (1), (5), (28), (29), and (34) along with defining, $v_{p,n} \equiv \alpha^p v_c = \alpha^p [v_n + I'(v_n)]$ and $v'_{p,n} \equiv v_{p,n} - I'(v_{p,n})$, yields

$$I(n) - I(n-1) = \frac{H_A(n)}{\alpha k} \lim_{r\to\infty} \prod_{p=1}^{r} \frac{H_A\left(v'_{p,n}\right)}{\alpha H_E\left(v'_{p,n}\right)} - 1. \tag{35}$$

If only one of $I(n)$ or $I(n-1)$ is known and the other unknown, and with INL assumed linearly interpolated, it can be shown that (35) is an *implicit* equation with only one unknown, $I(n)$ or $I(n-1)$, as the case may be, and has to be iteratively solved. However, the solution for most values of n is even easier when one considers the approximation shown in (36), valid at $|n| \gg I_{\max}$, maximum magnitude of INL. Equation (36) is an *explicit* equation, wherein the quantity on the right-hand side (RHS) is independent of the quantity on the left-hand side (LHS), letting the RHS to be directly evaluated. Generally speaking, the higher the linearity of the uncorrected ADC, the smaller the value of $I_{\max}$ and the more suitable is (36) for calibration

$$D(n) \approx \frac{H_A(n)}{\alpha k} \lim_{r\to\infty} \prod_{p=1}^{r} \frac{H_A(\alpha^p v_n)}{\alpha H_E(\alpha^p v_n)} - 1. \tag{36}$$

Iteration, using the solution of (36) as the initial guess, may be needed only when $|n|$ is close to zero, since for a high-end ADC $I_{\max}$ is typically from less than 1 LSB units to a few LSB units.

Starting from $I(0) = 0$ and using (35) and/or (36), the values of $I(1)$, $I(2)$, and so on can be determined successively, and so are the values of $I(-1)$, $I(-2)$, and so on, in that order.

Once the nonidealities have been estimated, the final output, corrected for both offset error and static nonlinearities, is given by using (1) and transforming back the coordinates.

$$v_c = v_n - V_{\text{offset}} + \frac{I\left(n - 1 - \frac{V_{\text{offset}}}{\Delta}\right) + I\left(n - \frac{V_{\text{offset}}}{\Delta}\right)}{2}. \tag{37}$$

Linear interpolation is applied wherever needed. The analysis made in this section is valid for most situations and is relatively independent of the resolution of the ADC, as long as the histograms contain enough hits to provide necessary smoothness to the amplitude-distribution curve. The assumptions made about the INL profile, leading to some simplifications, are also valid in most situations, when there are no missing codes. The odd exception too only needs simple iterative solutions to estimate DNL around the offset value. Implementation of (37) for each n generates the required LUT for error correction.

D. Step-Wise Summary of the Calibration Procedure

The online calibration of ADC is constituted by steps 1–7 listed below, which are repeated again and again, in the same order, for continual error correction. The procedure is diagrammatically shown in the flowchart of Fig. 6.

1) The mismatch-estimation phase is first run with $\alpha = 1$ (by setting the switch 'S' in Fig. 7 to the "Mismatch Estimation" position). After constructing and storing output histograms from a large number of samples, the mapping between each of the output levels of ADC and the corresponding portions of output levels of E-ADC is determined and the information stored in the memory. (In order to save on memory space, mismatch-estimation phase is run first, unlike the order in which the theory has been presented.)
2) ADC and E-ADC are reconfigured for the nonlinearity-estimation phase, by setting $\alpha \approx 0.5$ (by setting the switch 'S' in Fig. 7 to "nonlinearity estimation" position). Again, output histograms are constructed and stored from a large number of samples.
3) Based on the information stored in step 1), the histograms generated in step 2 are modified so as to effectively match E-ADC with ADC, and stored back.
4) The offset error of ADC is determined, and the origins of the histograms generated in step 3 are shifted to this offset value. This completes the task of pre-conditioning the output histograms.

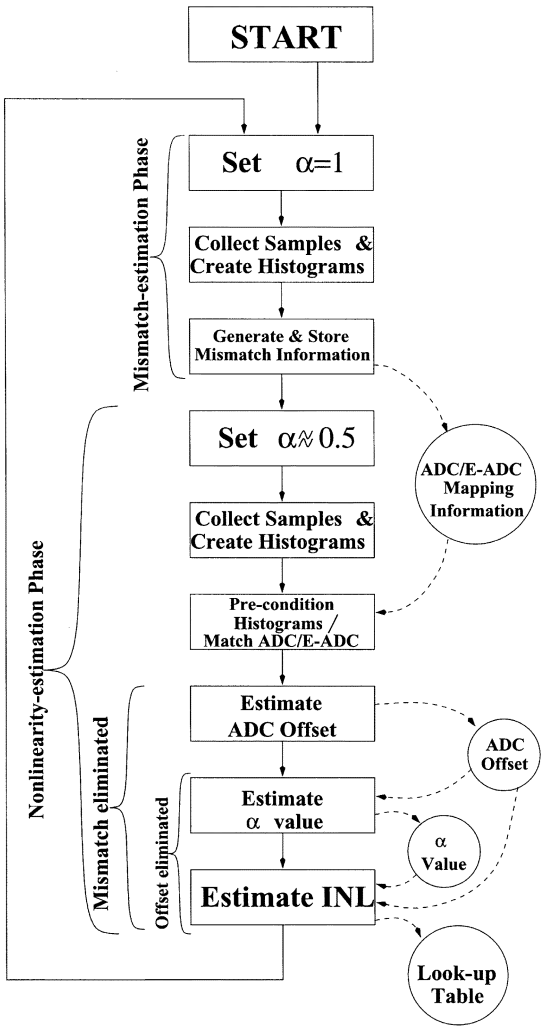

Fig. 6. Flow diagram for the calibration procedure.

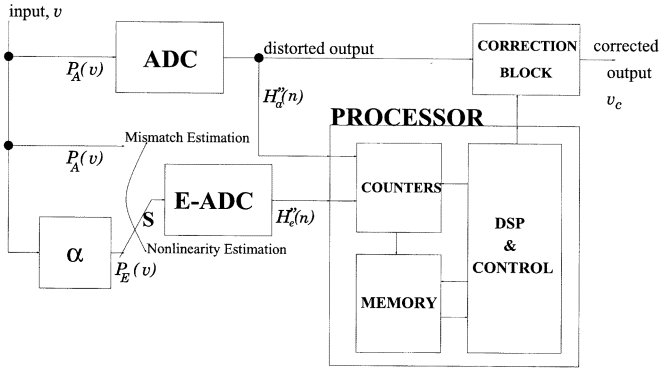

Fig. 7. Complete calibration scheme.

5) The *actual* value of the attenuator gain α is then accurately determined using the data stored.
6) The INL values are successively determined from the known value $I(0) = 0$ first for $n \geq 1$ and then for $n \leq -1$.
7) An LUT is generated and written into the "Correction Block" (Fig. 7) with an entry for each output level of ADC, based on its estimated offset error and static nonlinearities.

The duration of the calibration cycle depends on the time required to generate code-density histograms of sufficient hit-count as well as the time required to process the collected and stored data. The higher the quality of the ADC and/or calibration is, the higher the number of hits required for accurate estimation of errors, and so, the higher the time required to generate the histograms. The higher the resolution of the ADC, the higher is the time required to process collected data.

It is generally desired to minimize the duration of a single calibration cycle in order to minimize aging effects. However, the test-time (time period of a calibration cycle) during the online calibration described in this paper is many orders of magnitude less than the duration between two successive calibration cycles of any practicable offline calibration. Moreover, test-time in online calibration does not mean an interruption to real-time data conversion for the duration specified by test time, since the ADC is never interrupted from its intended activity.

V. Circuit-Overhead Estimation

The overhead circuitry required for the implementation of the online calibration scheme are mainly the following.

A. An Extra ADC

In this paper, the analysis has been presented for the case when this extra ADC is nominally identical (allowing mismatch) to the ADC to be calibrated. However, a lower resolution ADC may be used instead, thus achieving a *coarser* calibration, in applications where it suffices. The calibration procedure remains essentially the same in this case too, but the equations used then appear as though the resolution of the ADC to be calibrated is same as that of the lower resolution extra ADC.

B. An Analog Attenuator

The best implementation of a linear analog attenuator for voltage signals is as a voltage divider of nominal attenuation 0.5, implemented using two *matched* resistors of same value.

C. Counters and Memory

The calibration method presented in this paper is based on building code-density histograms. This requires counters to keep count of the number of hits on each output level of both the ADCs. If the ADCs are q-bit and if the maximum number of hits possible on any output level during a calibration cycle is such that the hit-count can be accommodated in d bits, then storing the histograms needs a maximum of $2d.2^q$ bits of storage space for both ADCs. The storage of mismatch information requires a maximum of $[x + y].2^q$ bits of space, where x and y respectively represent the maximum number of bits required to store the position of e_a (as the difference between a and e_a) and the value of f_a for any given a (refer to Section IV-A). In addition, the LUT for error correction requires $b.2^q$ bits of storage space for storing error values (max-

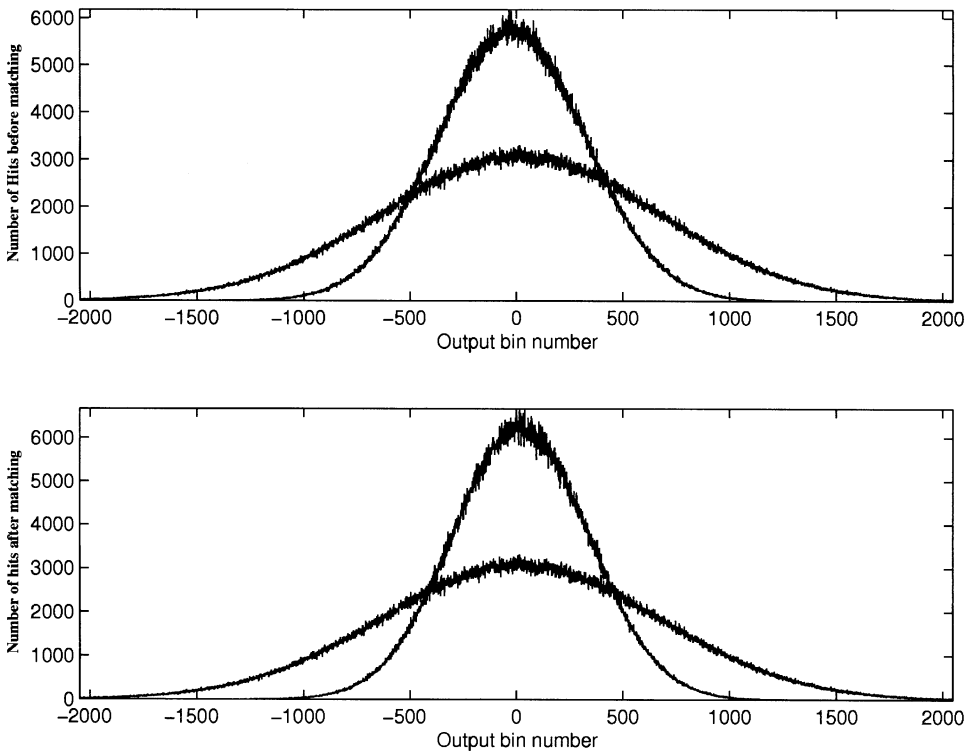

Fig. 8. Histograms before and after matching E-ADC with ADC (taller ones correspond to E-ADC). The smallness of nonidealities is reflected in the difficulty to discern the differences between the two figures with naked eye.

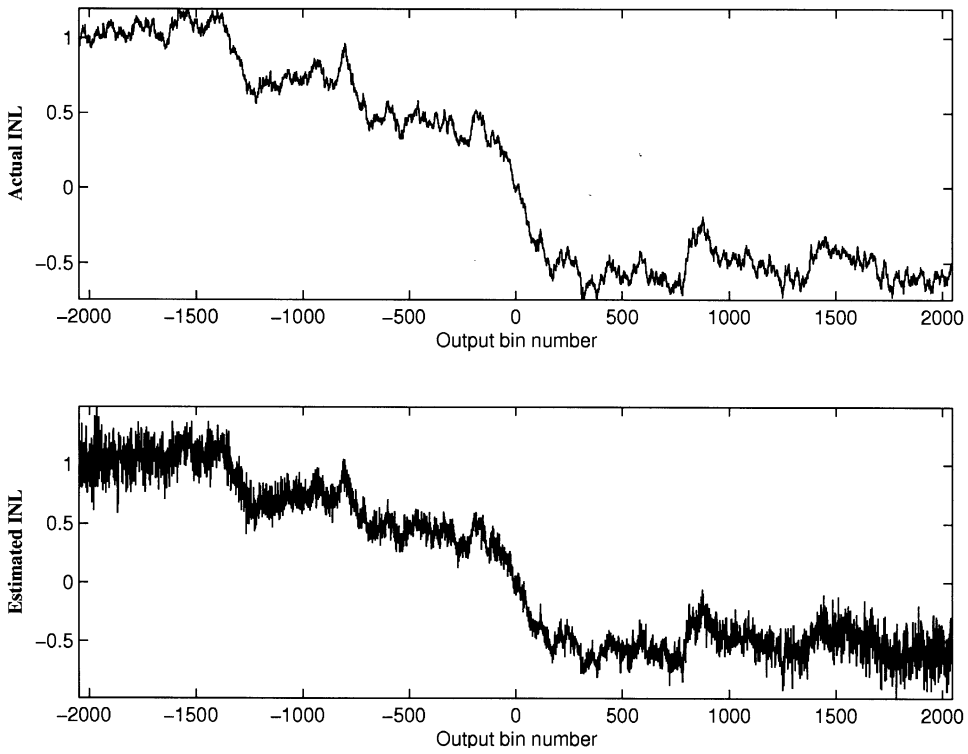

Fig. 9. ADC's modeled (actual) and estimated INL.

imum error value size is b bits) at each of the 2^q output levels. It all adds up to a storage space requirement of $2^q[2d+x+y+b]$ bits. It is possible to design a good calibration scheme for ADC resolutions up to 14 b with less than 1 million bits (128 KB) of storage space.

D. Switches and Associated Control Circuitry

A simple network of switches and associated control circuitry is needed to switch between mismatch-estimation and nonlinearity-estimation phases. Their contribution to the circuit overhead is small.

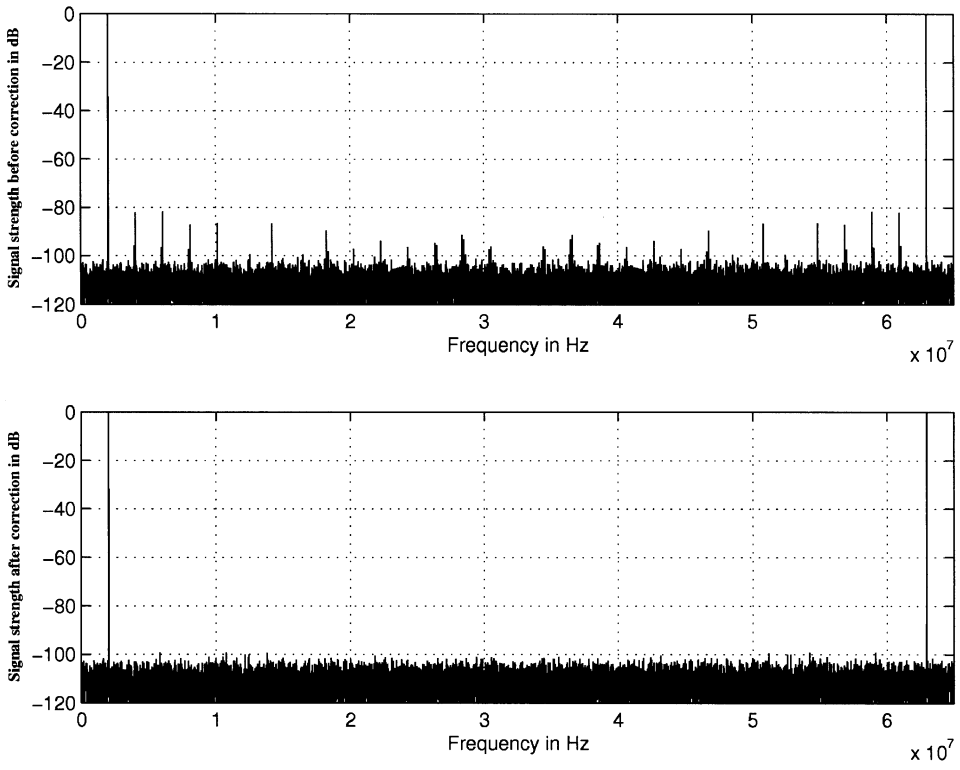

Fig. 10. Spectrum of ADC output before and after correction.

E. Digital Signal Processor

Since all the operations performed by the digital signal processor (DSP) block are basic arithmetic operations, as can be observed from the various equations in Section IV, a simple DSP block capable of doing these operations will suffice.

The major cost of the proposed technique is the silicon area for the second ADC. Doubling the analog section can be acceptable in future systems-on-chip where the analog part will be a small fraction of the entire chip. The required processing asks for a limited digital part that, possibly, can be incorporated on the on-board DSP.

VI. Simulation Results

MATLAB simulations were performed to validate the scheme. Both ADC and E-ADC were modeled as 12-b ADCs, with offset errors of $+20$ and -22 LSB units, respectively. Their DNL errors were generated randomly and separately such that they followed a normal distribution of mean zero and standard deviation 0.1 LSB units. This resulted in different INL errors on ADC and E-ADC. More mismatch was introduced by introducing different ADC gains—0.95 for ADC (gain error of -5%) and 1.03 for E-ADC (gain error of $+3\%$). The value of α used was 0.494. In each of the mismatch estimation and nonlinearity estimation phases, a total of 5×10^6 input samples were processed, with the input NADF following a normal distribution of mean zero and standard deviation $F/6$, where F represents the size of both ADCs' dynamic ranges, which are nominally from $-F/2$ to $F/2$. F was set to unity.

First, the mismatch-estimation phase (with $\alpha = 1$) was run, and the mismatch information stored. Then, during the nonlinearity-estimation phase (with $\alpha = 0.494 \approx 0.5$), the histograms of ADC and E-ADC were plotted and then preconditioned to effectively eliminate mismatch, using the mismatch information stored. The histograms before and after matching are shown in Fig. 8.

The offset of ADC was then calculated to be $+19.86$ LSB units (actual value is $+20$ LSB units). The histograms were then shifted to the offset value and α was calculated as 0.4940486 (actual value is 0.494), using $M = 8$ for averaging. INL at each output level was then determined successively, starting from the zeroth level and traveling toward either end of the ADC's dynamic range. The infinite product in (35) was approximated by the product of the first 25 factors. The INL error modeled into the ADC and the INL error estimated by this scheme are shown in Fig. 9. It may be noted that the error in INL estimation is higher toward the ends of the dynamic range. This is because of the choice of the input signal NADF modeled in the simulation. Because of fewer number of samples toward the ends of the dynamic range, the quantization error could not be eliminated up to the desired extent there, leading to higher estimation error. However, since the input signal was mostly restricted to the center of the dynamic range in this case, higher error at its ends would not hurt much. This, intrinsically, is the beauty of this scheme, whose accuracy is higher where it is required the most.

An LUT for correction was generated using the estimated offset and INL. A worst-case performance scenario was simulated by using a test-signal with an amplitude distribution which has higher hit-count toward the either end of the dynamic range

than at its center (unlike the amplitude-distribution used to estimate the errors). Accordingly, a single-tone sinusoidal input of amplitude $= 0.4995$ and frequency $= 2.03$ MHz was fed to the ADC. The sampling rate of ADC was chosen as 65 Msamples/s. Since the method corrects static limitations only, no finite speed degradation has been considered. Therefore, the used sampling frequency just reflects a possible realistic operative condition. The fast Fourier transform (normalized to 0 dB) of the ADC's output using 16384 samples, and applying a Blackman windowing function, was plotted before and after correction as shown in Fig. 10. An improvement in the spurious-free dynamic range (SFDR) of at least 20 dB, over a value of 82 dB for the uncorrected output, was achieved using this calibration scheme.

VII. Conclusion

A scheme for the online calibration of an ADC using output code-density histograms has been proposed. The suitability of the scheme for calibrating high-end ADCs has been demonstrated. The circuit-overhead estimation has been presented in detail, outlining possible tradeoffs. An improvement in SFDR by at least 20 dB from its value of over 80 dB for the uncorrected ADC output has been achieved.

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