

Noise in mixed continuous-time switched-capacitor sigma-delta modulators

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Indexing terms: Noise, Modulators

Abstract: It is commonly accepted that oversampling/noise-shaping is the most suitable technique for implementing high-resolution data converters in MOS technologies. Most existing modulators use switched-capacitor (SC) techniques because they provide a highly controllable design. When compared to continuous-time (CT) techniques, SC techniques have two main drawbacks: settling time limitation and thermal noise folding. In this paper the performance of mixed continuous-time/switched-capacitor (CT-SC) and SC modulators is compared by analytically evaluating the thermal and jitter noise contributions. Relationships are derived which define the conditions for designing mixed modulators with lower levels of noise power than their SC counterparts. The main conclusion is that in mixed modulators the thermal noise can be significantly reduced, while the jitter noise could be a severe limit on the realisation of high resolution converters.

1 Introduction

Recent advances in analogue-to-digital (A/D) conversion techniques indicate that oversampling/noise-shaping is the most suitable approach for designing high-resolution data converters [1-6]. As far as the implementation technique is concerned, SC circuits have been preferred to CT circuits for two reasons. First, the achievable accuracy is good enough for the applications envisaged and, secondly, several techniques exist that permit compensation for the typical nonideal effects of active and passive components. Moreover, SC integrators have a time constant which can be easily changed by moving the sampling frequency, without necessitating further circuit design. This is a very useful feature from the point of view of general purpose design as well as for testing flexibility.

A block diagram of a generic noise-shaping modulator is shown in Fig. 1. For the case of a noise transfer function like $(1 - z^{-1})^L$, eqn. 1 gives the inband quantisation noise power P_Q of the modulator as a function of modulator order L , quantiser resolution N , oversampling ratio

M , and quantiser output levels $\pm \Delta$.

$$P_Q = \frac{4}{3} \frac{\Delta^2}{2^{2N}} \frac{\pi^{2L}}{2L+1} \frac{1}{M^{2L+1}} \quad (1)$$

This relationship indicates that a gain in resolution of $(L + 1/2)$ bit per octave of oversampling ratio and 1 bit per bit of accuracy in the quantiser can ideally be achieved with this technique.

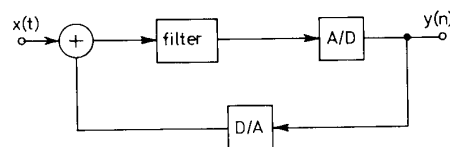


Fig. 1 Block diagram of oversampled noise-shaping modulator

The resolution, however, is limited for two reasons: the maximum oversampling frequency allowed by the op-amps and the thermal noise due to the amplifiers and the switches. As we found in a recent work [7], for each modulator order there is an oversampling ratio M_L above which the circuit behaves as a common oversampled circuit, i.e. the shaping of the quantisation noise is no longer effective because nonshaped thermal noise prevails. As consequence, above M_L the increase in the signal-to-noise-ratio (SNR) is limited to 3 dB per octave of oversampling ratio. This limitation is valid up to the speed limit of the circuit, after which there is a decrease instead of an increase in the SNR.

To overcome these drawbacks, some authors have proposed the mixed CT-SC approach [8]. Basically, it involves using a CT circuit as the first integrator, and using SC circuitry to implement the other integrators. This shifts, the sampling operation to the second stage, thus strongly reducing the noise aliasing effects as well as the anti-aliasing requirements.

The main objective of this paper is to compare the performance of mixed and SC modulators through an analytical evaluation of the noise source contributions. For a common CT integrator we derive relationships which allow the effects of thermal and jitter noise in mixed modulators to be expressed. From these relationships together with those obtained in the SC case, the design conditions to obtain lower noise in mixed modulators will be determined. We show that the mixed CT-SC

Paper 9009G (E10), first received 23rd December 1991 and in revised form 26th May 1992

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The ECC-Joint Research Centre and Piano Nazionale della Microelettronica provided financial support for this research.

technique has the potential to reduce the thermal noise limit imposed on SC modulators by the sampling process, and also that clock jitter can be responsible for a severe deterioration of the noise performance of mixed modulators.

2 Mixed continuous-time switched-capacitor modulator

Let us consider, for simplicity's sake, the schematic diagram of the mixed CT-SC second-order sigma-delta modulator illustrated in Fig. 2. The first integrator is a

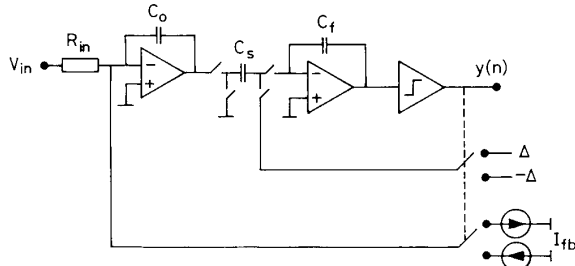


Fig. 2 Schematic diagram of mixed CT-SC second-order $\Sigma\Delta$ modulator

continuous-time active circuit with voltage V_{in} and the switched current source I_{fb} as input signals. The resistance R_{in} and capacitor C_o together define the time constant for the input signal, $R_{in}C_o$, while the capacitor C_o alone works as a current integrator for the feedback signal I_{fb} . The second integrator is of a switched-capacitor type, whose time constant is determined by capacitor C_f , the sampling capacitor C_s , and the sampling frequency F_s . Here the feedback signal is represented by $\pm\Delta$. Although the example in Fig. 2 uses an RC-active circuit as the first integrator, other continuous-time implementations can be adopted [9]. In these cases the following discussion also holds, apart from some minor changes.

Let us assume that the absolute value of the integral of the feedback current $I_{fb}(t)$ is independent of the particular time-slot we are considering and equal to Δ . This is the same as assuming, for each time-slot, the following relation

$$\int_{(n-1)T_s}^{nT_s} \frac{I_{fb}(t)}{C_o} dt = \frac{1}{C_o} Q_{fb}(n) = \pm\Delta \quad (2)$$

where $\pm\Delta$ also stands for the equivalent feedback voltage step added to the integrating capacitor during the time interval $[(n-1)T_s, nT_s]$. Eqn. 2 can be used to model the modulator as illustrated in Fig. 3. This is now

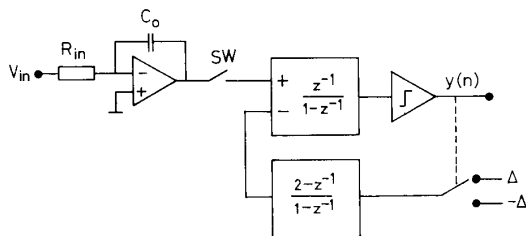


Fig. 3 Modified schematic diagram of mixed CT-SC second-order $\Sigma\Delta$ modulator

composed of a CT integrator cascaded with a sampled-data circuit. The switch SW between the CT and SC sections represents the sampling operation that takes place at the input of the second integrator. The feedback signal is directly applied to the second integrator with a transfer function which is changed accordingly. In this way the quantisation noise is only processed in the sampled-data domain with a transfer function which is exactly equal to that of its equivalent SC modulator. Although the circuit in Fig. 3 does not have a physical implementation because the first integrator is in an open-loop configuration, it is very useful in evaluating the noise performance of a mixed modulator.

To obtain a signal transfer function equivalent to that of a fully-SC modulator, the following condition between the CT and the SC integrators has to be met

$$I_{CT}(j\omega) = I_{SC}(e^{j\omega}) \quad -\pi F_s \leq \omega < \pi F_s \quad (3)$$

where $I_{CT}(j\omega)$ and $I_{SC}(e^{j\omega})$ are the frequency responses of ideal CT and SC integrators, respectively. Indeed, since

$$|I_{CT}(j\omega)| = \frac{1}{\omega R_{in} C_o} \quad (4)$$

and in the band of interest

$$|I_{SC}(e^{j\omega})| = \frac{1}{\omega T_s} \quad \text{for } \omega T_s \ll 1 \quad (5)$$

expr. (3) implies $R_{in}C_o = T_s$. Eqn. 5 is the design condition for the time-constant of the CT integrator.

3 Thermal noise

A relationship for the thermal noise in mixed CT-SC modulators is now determined. Flicker noise will not be considered, because techniques exist which can reduce its effects [8, 10].

Thermal noise is one of the first fundamental limitations when designing high-resolution A/D converters. In particular, for $\Sigma\Delta$ modulators a critical parameter is the noise of the first integrator, because it is not shaped by the modulator, unlike the quantisation noise. As shown in Fig. 4, the noise sources that contribute prin-

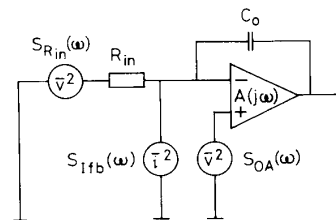


Fig. 4 Thermal noise sources in a continuous-time integrator

cipally to the overall thermal noise power are the input resistance, the amplifier broad-band noise and the feedback current source thermal noise. The bilateral power spectral density associated with each of these sources is

$$S_{R_{in}}(\omega) = 2kTR_{in} \quad (6)$$

$$S_{O_A}(\omega) = 2kTR_{eq} \quad (7)$$

$$S_{I_{fb}}(\omega) = 2kTG_{eq} \quad (8)$$

where R_{in} is the input resistance and R_{eq} and G_{eq} are the equivalent noise resistance and conductance of the operational amplifier and the current source, respectively.

Consider now a real integrator built up from a single-pole operational amplifier whose frequency response $A(j\omega)$ is given by

$$A(j\omega) = \frac{A_o}{1 + j\omega\tau} \quad (9)$$

The two noise sources $S_{oA}(\omega)$ and $S_{Ifb}(\omega)$ can be referred to the input of the integrator, allowing the input-referred total noise power spectral density, $S_{in}(\omega)$, to be expressed as

$$S_{in}(\omega) = S_{Rin}(\omega) + S_{oA}(\omega)|H_{oA}(j\omega)|^2 + R_{in}^2 S_{Ifb}(\omega) \quad (10)$$

where $H_{oA}(j\omega)$ stands for the frequency response which applies to the noise source $S_{oA}(\omega)$ when it is transferred from the op-amp noninverting terminal to the output and is then referred to the input of the integrator. Assuming that the unity-gain frequency of the integrator, ω_o ($\omega_o = 1/R_{in}C_o$), is much smaller than the gain-bandwidth product of the amplifier, ω_u ($\omega_u = A_o/\tau$), $H_{oA}(j\omega)$ can be written as

$$H_{oA}(j\omega) = \frac{1 + j\omega R_{in}C_o}{1 + j\omega\tau/A_o} \approx 1 \quad \text{for } \omega \leq 1/R_{in}C_o \quad (11)$$

This simplification is valid for the frequencies of interest. From eqns. 6–11 the input-referred noise power spectral density can be written as

$$S_{in}(\omega) = 2kTR_t \quad (12)$$

where

$$R_t = R_{in} + R_{eq} + R_{in}^2 G_{eq} \quad (13)$$

is the equivalent input-referred noise resistance of the modulator.

To take the sampling operation into account we can refer to the simplified model shown in Fig. 5. The noise

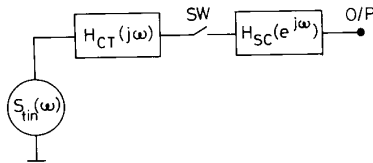


Fig. 5 Simplified block diagram for noise evaluation in mixed CT-SC modulators

power spectral density $S_{in}(\omega)$ is primarily filtered by the continuous-time integrator whose frequency response is now

$$H_{CT}(j\omega) = -\frac{A_o}{1 + j\omega(\tau + A_o R_{in} C_o)} \approx -\frac{A_o}{1 + j\omega A_o R_{in} C_o} \quad \text{for } \tau \ll A_o R_{in} C_o \quad (14)$$

and is then sampled and processed in the sampled-data domain by the high-pass transfer function

$$H_{SC}(z) = z^{-1}(1 - z^{-1}) \quad (15)$$

Fig. 6 shows the Bode diagram of the real integrator frequency response $H_{CT}(j\omega)$ together with the power spectral density $S_{in}(\omega)$. As is well known, the finite op-amp DC gain gives rise to a nonzero pole frequency $\omega_c = 1/A_o R_{in} C_o$, while maintaining the unity-gain frequency $\omega_o = 1/R_{in} C_o$. It is now clear that, before sampling, the

noise spectra is lowpass filtered within the cut-off frequency ω_c which is much smaller than the sampling frequency F_s ($R_{in} C_o$ has been set to T_s). This condition guarantees that the contribution of the high frequency

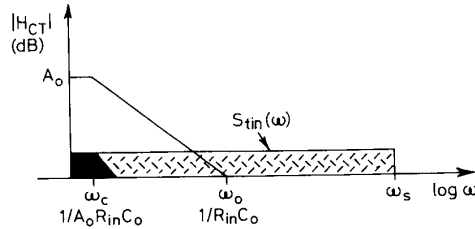


Fig. 6 Bode diagram of integrator frequency response and total thermal noise power spectral density

noise aliased down into the baseband is negligible. Since no aliasing is present the noise power spectral density at the output of the modulator can thus be written as

$$S_{Th}(\omega) = S_{in}(\omega) |H_{CT}(j\omega)|^2 |H_{SC}(e^{j\omega})|^2 \quad -\pi F_s \leq \omega < \pi F_s \quad (16)$$

that integrated into the signal band, B_o , gives the following noise power

$$P_{Th} = 2kTR_t(2B_o) \quad (17)$$

This equation indicates that the thermal noise power in mixed modulators is the same as for a true CT circuit in which no folding effects are present. For a given signal bandwidth B_o , the thermal noise power is constant, i.e. it is not a decreasing function of the oversampling ratio M as happens in SC modulators (3 dB per octave of M).

4 Jitter

Jitter is the intrinsic uncertainty in the time-instant of the clock transitions. Continuous-time modulators are sensitive to jitter because they use the time-slot length as a parameter to convert current into voltage. As shown in Fig. 7a, we consider the jitter as a random phenomena in

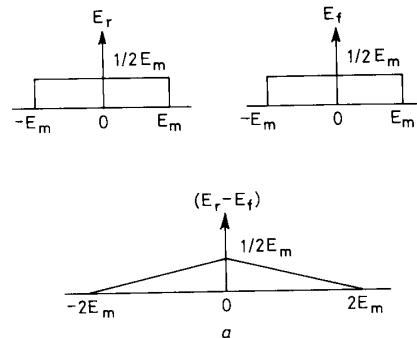


Fig. 7

a Probability density function of E_r , E , and $(E_r - E_f)$
b Equivalent circuit for analysis of clock uncertainty effects in continuous-time integrators

which the rise and fall transition instant errors, E_r and E_f , are assumed to be independent and uniformly distributed random variables [11, 12]. They are defined in a range $[-E_m, E_m]$, where E_m is the maximum deviation in seconds from the ideal clock transitions. Let us consider the CT integrator in Fig. 7b whose integrating time slot, T_{int} , is equal to a half clock period ($T_{int} = 1/2F_c$). In ideal clocking conditions the voltage at the output of the integrator changes by $\Delta = (I_{fb}/C_o)T_s/2$ per clock period. Owing to clock uncertainty, at the end of the integration period error samples of magnitude

$$\Delta_E = (E_f - E_r)I_{fb}/C_o \quad (18)$$

result. These error samples can be considered in the sampled data domain, as was the ideal term of the integral of the feedback current. The resulting distribution for Δ_E is triangular in $[-2E_m, 2E_m]I_{fb}/C_o$ (see Fig. 7), and has a corresponding variance of $\sigma^2 = (2/3)(E_m I_{fb}/C_o)^2$. Since Δ_E is a random process with a sampling frequency of F_s , the corresponding power spectral density is uniform

$$S_{jitter}(f) = (8/3) \Delta^2 E_m^2 F_s \quad -F_s \leq f < F_s \quad (19)$$

where it has been assumed that $\Delta = (I_{fb}/C_o)T_s/2$. Since this noise source is not shaped on its way to the modulator output, the resulting in-band noise power is therefore

$$P_{jitter} = (8/3) \Delta^2 E_m^2 (2B_o)^2 M \quad (20)$$

This equation indicates that in-band jitter noise power increases by 3 dB per octave of oversampling ratio, and 6 dB per octave of increase of either the uncertainty in the time instant of the clock transitions or the signal bandwidth. For example, oversampling ratios in the range 64–512 and clock uncertainty values in the range 1–100 ps lead to a noise power which lies in the range (-125) – (-76) dB ($\Delta = 1$ V, $B_o = 22$ kHz).

5 Comparison between SC and mixed modulators

In the preceding sections we analysed two of the possible limits in the design of high-resolution mixed CT-SC modulators: the thermal noise associated with the first integrator and the jitter noise of the clock generator. Each of these contributions as well as the quantisation noise P_Q for different modulators orders ($L = 2, 3$ and 4) are plotted as a function of the oversampling ratio M (see Fig. 8). All the modulators use 1 bit quantisers with quantisation levels $\Delta = \pm 1$ V, the equivalent input noise resistance R_i has been set to 10 k Ω , and a 22 kHz signal bandwidth has been assumed. As can be seen, for each modulator order there can be a maximum of three

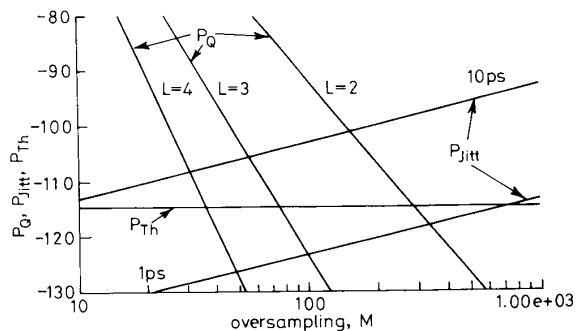


Fig. 8 Quantisation, P_Q , jitter, P_{jitter} , and thermal, P_{Th} , noise powers against M for 1-bit mixed CT-SC second-order $\Sigma\Delta$ modulators
 $B_o = 22$ kHz, $\Delta = \pm 1$ V, $R_i = 10$ k Ω , $E_m = 10$ ps and 1 ps

working regions: a noise-shaping limited region where the quantisation noise predominates, $P_Q > P_{jitter}$, P_{Th} , a thermal noise limited region where the thermal noise predominates, $P_{Th} > P_Q$, P_{jitter} , and a jitter limited region in which the jitter noise prevails, $P_{jitter} > P_Q$, P_{Th} . For the same conditions given for the curves in Fig. 8 and a clock uncertainty parameter of 10 ps, the plot in Fig. 9 shows the maximum achievable resolution as a function of the oversampling ratio for three different mixed modulators.

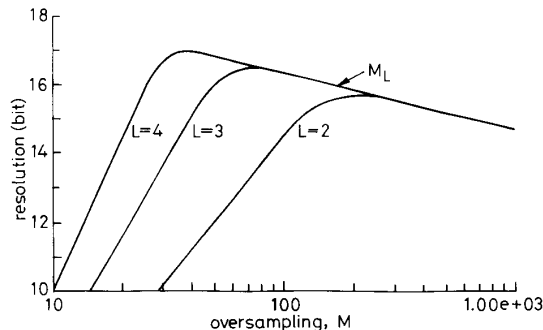


Fig. 9 Maximum achievable resolution against M for 2nd, 3rd and 4th order 1 bit mixed CT-SC $\Sigma\Delta$ modulators
 $B_o = 22$ kHz, $\Delta = \pm 1$ V, $R_i = 10$ k Ω , $E_m = 10$ ps

The input signal is assumed to be sinusoidal with the amplitude equal to Δ . For each modulator we identify an oversampling corner value above which the resolution decreases by 1/2 bit per octave of M , since the jitter noise predominates. This oversampling corner decreases with the modulator order, but higher resolutions can be achieved. There is also an oversampling factor M_L above which all the modulators behave similarly.

The settling error in the SC integrators should also be taken into account, a fact that by itself should impose a maximum sampling frequency [7]. This error, however, gives an appreciable contribution only for a very high oversampling ratio since errors added in the integrators following the first are filtered by the modulator.

We now compare the results obtained with those for SC modulators [7]. Reference 7 states three relationships which define the main limitations of SC $\Sigma\Delta$ modulators. They are: the quantisation noise power, P_Q , reported in eqn. 1, the thermal noise power

$$P_{Th} = \frac{10 kT}{3} \frac{1}{C_s M} \quad (21)$$

where C_s stands for the sampling capacitor in the first integrator, and the settling-induced noise power

$$P_{St} = K_{int} \frac{1}{M} e^{-(g_m/2B_o M C_s)} \quad (22)$$

Here g_m is the transconductance of the amplifier and K_{int} is a constant which depends on the maximum output current of the amplifier, on the ratio between the sampling and integrating capacitors and on the quantisation step. Fig. 10 plots these three noise contributions for the typical design conditions of a high-resolution 1 bit second-order SC $\Sigma\Delta$ modulator.

Eqns. 17 and 21 show that to have a mixed modulator with a thermal noise power which is lower than an SC one, the following relation has to be met

$$R_i = \frac{5}{3} \frac{1}{F_s C_s} \quad (23)$$

This equation states that the equivalent noise resistance, R_t , must be lower than approximately twice the equivalent resistance of a switched-capacitor branch, $1/(F_s C_s)$. For example, with a signal bandwidth of 22 kHz, an

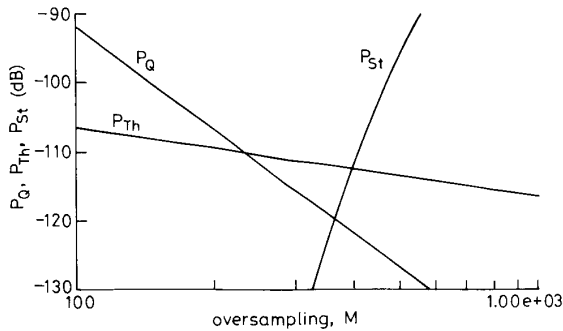


Fig. 10 Quantisation, P_Q , settling, P_{st} , and thermal, P_{Th} , noise powers for 1 bit SC second-order $\Sigma\Delta$ modulators [7]

equivalent noise resistance of 20 k Ω gives a thermal noise power of ≈ -110 dB. Comparatively, the same noise performance could be achieved with a SC modulator whose oversampling ratio and sampling capacitor are as high as 256 and 6 pF, respectively.

From eqns. 20 and 21 we find that the condition to obtain jitter noise in CT modulators which is smaller than kT/C noise in SC modulators is ($\Delta = 1$)

$$E_m(\text{ps}) \leq \frac{70}{[C_s(\text{pF})]^{1/2}} T_s(\mu\text{s}) \quad (24)$$

From this relationship it follows that to design a mixed modulator with the same noise performance as a SC modulator whose sampling frequency and capacitor are 10 MHz and 6 pF, respectively, a clock uncertainty coefficient as low as 3 ps would be required.

Another important parameter in high-resolution sigma-delta A/D converters, not considered here, is the linearity feature. It is well known that the standard CMOS processes used for these applications employ active and passive components whose linearity characteristic is inadequate to achieve the high accuracy required. However, to avoid a quality degradation for high input levels, the linearity performance of such converters should not be much lower than the dynamic range requirement.

The main sources of distortion in SC modulators are the nonlinear DC-gain characteristic of operational amplifiers, the signal-dependent clock feedthrough and the voltage coefficient of integrated capacitors. The major contribution is, however, due to operational amplifiers. Integrated capacitors have a linearity feature which is one or more orders of magnitude smaller, while techniques exist which allow rather good compensation for clock feedthrough distortion. As far as mixed modulators are concerned, the linearity performance is a more crucial parameter than for SC circuits. Unlike SC modulators, the amplifier in the first integrator of mixed modulators has to deliver a dynamic current to the output, degrading the overall performance.

As a final consideration, it is worth noting that, besides the high value of integrated capacitor and resistance tolerances, integrated resistances have a voltage coefficient which is an order of magnitude higher than that of integrated capacitors. All these drawbacks make the full monolithic implementation of mixed modulators difficult.

6 Conclusions

We have analysed the two main factors which determine the maximum achievable resolution in mixed continuous-time/switched-capacitor $\Sigma\Delta$ modulators. Special attention has been paid to the analysis of the basic structure of a mixed modulator for which a simplified analytical model has been developed. Relationships have been derived for the thermal noise associated with the first integrator as well as for the jitter noise induced by the clock generator. The uncertainty in the clock transitions has been assumed to be a random and independent variable with uniform distribution. From the relationships derived, three working regions were identified in mixed modulators: first, a noise-shaping limited region in which the quantisation noise predominates, and thus a $6(L + 1/2)$ dB increase per octave of M is seen in the SNR; secondly a thermal limited region where thermal noise prevails and no increase is seen in the SNR; and finally, a jitter limited region in which the jitter noise prevails and a decrease of 3 dB per octave is seen. The main conclusion is that mixed modulators, apart from reducing anti-aliasing requirements, can also be designed to have very low levels of thermal noise power. Unfortunately, the uncertainty in the clock transitions could be responsible for a drastic degradation of the overall noise performance. The condition for having mixed modulators with a jitter noise power which is smaller than the kT/C noise power in SC modulators has also been determined.

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