# Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part II: Non-Constant Input

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***Abstract*—In this two-part paper, a design methodology for hardware reduction in digital delta-sigma modulators (DDSMs) based on bus-splitting and error masking is presented. Part I addresses Multi stAge noise SHaping (MASH) DDSMs with constant inputs; Part II focuses on error feedback modulators (EFMs) with time-varying inputs. In this paper, we address EFMs with DC inputs plus additive input least significant bit (LSB) dithering and show how hardware reduction can be achieved with minimal degradation of the output spectrum. We also address EFMs with sinusoidal inputs and show how bus-splitting and error masking techniques can be used to obtain a trade-off between the modulator complexity and the achievable signal-to-noise ratio.**

***Index Terms*—Bus-splitting, digital delta-sigma modulator (DDSM), nesting.**

## I. Introduction

THIS is the second part of a two-part paper that presents a design methodology for hardware reduction in digital delta-sigma modulators (DDSMs) based on bus-splitting and error masking. Part I of the paper considered Multi stAge noise SHaping (MASH) DDSMs with constant inputs [1]. Such systems have applications in fractional-N frequency synthesizers for generating fixed frequencies by modulating the instantaneous division ratio of a frequency divider. The design methodology in that case exploits knowledge of the positions of the tones. Part II of the paper considers error feedback modulators (EFMs) with time-varying inputs. The *positions* of the tones in the DDSM's output spectrum are typically unknown when the input is time-varying. In this case, the design methodology exploits knowledge of the *shape* of the noise floor.

In this work, we consider two different types of inputs. The first input we discuss consists of two components, namely a constant value and a pseudorandom 1-bit LSB dither signal [2]. In the fractional-N frequency synthesizer application, the presence of spurious tones in any part of the spectrum is highly objectionable as any nonlinearity in the implementation of the phase-frequency detector, charge pump, filter, VCO or divider can cause out-of-band tones to fold back into the baseband, thereby increasing the phase noise in the vicinity of the carrier [3], [4]. Therefore, it is crucial that the quantization noise introduced by the DDSM is white and independent of the modulator's input because strong correlations between the modulator input and quantization noise can lead to spurious tones in the output spectrum of the DDSM. The use of stochastic LSB dithering can impart these properties to the quantization noise, in certain cases, at the expense of a degradation in the phase noise of the PLL output [5]–[7]. Alternatively, a number of deterministic strategies have been proposed for minimizing spurious tones [8], [9].

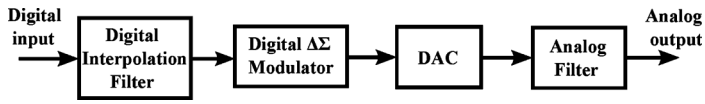


Fig. 1. Block diagram of a typical oversampling delta-sigma DAC.

The second type of input we consider is a digitized sinusoid because DDSMs are widely used in oversampling digital-to-analog converters (DACs) [10]. Fig. 1 shows a high level block diagram of a typical delta-sigma DAC, consisting of a digital interpolation filter, a DDSM, a DAC and an analog filter with a lowpass response [11]. The input digital signal, sampled at the Nyquist rate, is upsampled using a digital interpolator and the resulting bit sequence is passed to a DDSM which reduces the word length of the binary code. The output signal of the DDSM is converted to an analog signal in the DAC block and finally the analog output is low pass filtered to remove the out-of-band quantization noise.

The design of a DDSM for use in an oversampling DAC involves a number of trade-offs. Nonlinearity in the DAC can cause increased signal distortion at the output. The main advantage of one-bit DDSMs is the inherent linearity of the corresponding one-bit DAC. These modulators are not suitable for high speed data conversion because a large oversampling ratio (OSR) is required to achieve high resolution when the signal bandwidth of interest becomes large [12]. A large OSR restricts the circuit's bandwidth and increases its power dissipation. Once again, it is crucial that the quantization noise introduced by the DDSM is asymptotically white and independent of the modulator's input because strong correlations between the modulator input and quantization noise can lead to spurious tones in the output spectrum of the DDSM. In data converter applications, spurious in-band tones are undesirable because they degrade the signal-to-noise ratio (SNR). In the case of one-bit modulators, the white noise approximation is generally not valid [11].

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The use of a multibit DDSM reduces the OSR required to achieve a specific resolution. Multibit modulators produce fewer spurious tones and lower out-of-band quantization noise; this relaxes the analog post filtering requirements [13]. The main drawback of a multibit DDSM is the nonlinearity of the corresponding multibit DAC. This necessitates the use of linearization techniques such as dynamic element matching (DEM) to mitigate the consequences of the nonlinearity and to ensure that mismatches among the DAC elements do not corrupt the desired signal [14], [15]. In this paper, we focus on multibit digital delta-sigma modulation with sinusoidal inputs.

In order to ensure high performance, it is necessary to use high order modulators to obtain significant noise shaping in the signal band. High order DDSMs can be realized with interpolative or MASH architectures [11]. An $n$th order interpolative architecture typically incorporates a single quantizer and a single $n$th order discrete-time filter. For $n > 1$, interpolative modulators employing a one-bit quantizer require signal conditioning around the loop for stability control, which reduces the available dynamic range at the input. Applying a full-scale input to a high-order single bit DDSM causes the quantizer to be overloaded frequently, leading to severe distortion at the DDSM's output. The use of a multibit quantizer increases the achievable dynamic range for a higher order modulator by ensuring its stability over a larger input range [12]. In this work, we focus on the error feedback modulator architecture which is the simplest implementation of a delta-sigma modulator for a digital application. Prior work [16] has shown that this architecture does not experience quantizer overload if a $k$th-order FIR noise transfer function (NTF) is used in conjunction with a $(k+1)$-bit truncator.

In this work, we investigate a bus-splitting idea for implementing DDSMs with non-constant inputs, in which the digital input word to a high order DDSM is partitioned into a number of parts and the LSBs are processed by one or more low order DDSMs before being recombined with the MSBs. Our work has been inspired by the ideas of Norsworthy *et al.* [17] in which the data path of a multibit digital noise shaper is reduced by noting that noise shaping only needs to be performed on the lower few LSBs of an oversampled digital signal in order to be effective. The authors of [17] presented simulation results in which they compared the performance of a traditional single-stage noise shaper with their minimal multibit noise shaping architecture. They truncated the lower 8 bits of a 16-bit sine wave and passed the 8 LSBs through a second-order noise shaper before recombining them with the 8 MSBs. This was shown to produce a similar baseband noise floor to the traditional method of passing the entire 16 bits through the second order noise shaper. Schreier and Temes claim that "for sufficiently large OSR, the accuracy can be satisfactory" [11].

To date, the performance of bus-splitting combined with digital delta-sigma modulation has been evaluated based on insight, empirical observations and simulations. The goal of this paper is to formalize the method. In the case of an oversampling DAC, the wordlength of the modulator is typically defined by the output SNR specification; the wordlength in turn determines the power consumption and area. Reducing the wordlength usually degrades the SNR but also decreases the power consumption and area. In this work, we consider the components that contribute to the output SNR of a DDSM and show how these can be manipulated to reduce the overall complexity of the modulator with minimum degradation of the SNR. In particular, spectral shaping and masking techniques can be used to reduce the hardware requirements faster than the SNR; these can yield a design that is roughly 40% more efficient in terms of power and area.

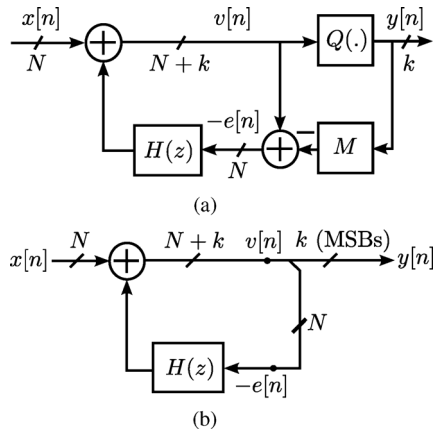


Fig. 2. (a) Block diagram of an $l$th order error feedback modulator (EFM$l$) and (b) its hardware implementation.

This paper is organized as follows. In Section II, we review the conventional EFM architecture. In Section III, we describe bus-splitting EFM architectures. In Section IV, we compare the conventional and bus-splitting dithered EFM architectures and develop a design methodology which ensures that the spectral performances of the bus-splitting architectures are comparable to the conventional design. In Section V, we consider an EFM with a sinusoidal input and explain how a trade-off between SNR and hardware complexity can be achieved.

## II. Conventional EFM Architecture

Fig. 2(a) shows the block diagram of an $l$th order error feedback modulator (EFM$l$) with integer valued signals $x[n], v[n], y[n]$, and $-e[n]$.

The input to the modulator is an $N$-bit digital word. The truncation quantizer in the EFM implements the following operation:

$$y[n] = \left\lfloor \frac{v[n]}{M} \right\rfloor \tag{1}$$

where $\lfloor x \rfloor$ denotes the largest integer less than or equal to $x$ and $M = 2^N$ is the step size of the quantizer in the EFM. In the Z-domain, we can write the output of the EFM $Y(z)$ in terms of the input $X(z)$ and the quantization error $E(z)$ as

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E(z) \tag{2}$$

where $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ are the signal and noise transfer functions, respectively. Assuming that the feedback filter is of the form $H(z) = 1 - (1 - z^{-1})^l$, the output is given by

$$Y(z) = \frac{1}{2^N}X(z) + \frac{1}{2^N}(1 - z^{-1})^l E(z). \tag{3}$$

Fig. 2(b) shows the hardware implementation of the EFM$l$. The $k$-bit quantization is achieved by taking the $k$ MSBs of $v[n]$. The discarded LSBs, representing the negative of the quantization error $(-e[n])$, are fed back and summed with the input. An EFM is guaranteed to be free of quantizer overload provided that a $k$-bit truncator is used in conjunction with a $(k-1)$th order loop filter [16].

## III. Bus-Splitting Architectures

Fig. 3(a) shows the block diagram of a conventional $N$-bit third-order error feedback modulator (EFM3). In this case, the EFM3 processes the entire $N$ bits of the input. Consider the architectures in Figs. 3(b) and (c), to which we will refer as a bus-splitting 1-3 EFM3 and a bus-splitting 2-3 EFM3, respectively. In these cases, the digital input word is divided into two parts: the $N_{\rm MSB}$ most significant bits and the $N_{\rm LSB}$ least significant bits. The $N$-bit input can be written as

$$X = X_{\rm MSB} \cdot 2^{N_{\rm LSB}} + X_{\rm LSB} \tag{4}$$

where $X_{\rm MSB}$ and $X_{\rm LSB}$ correspond to the MSBs and LSBs, respectively, and

$$N = N_{\rm MSB} + N_{\rm LSB}. \tag{5}$$

Consider the bus-splitting architecture of Fig. 3(d), to which we will refer as a *nested* bus-splitting 1-2-3 EFM3. In this case, the digital input word is first divided into two parts: the $N_{\rm MSB}$ most significant bits, and the remainder. The latter is then further subdivided into the $N_{\rm ISB}$ intermediate bits and the $N_{\rm LSB}$ least significant bits. The $N$-bit input can be written as

$$X = X_{\rm MSB} \cdot 2^{N_{\rm LSB}+N_{\rm ISB}} + X_{\rm ISB} \cdot 2^{N_{\rm LSB}} + X_{\rm LSB} \tag{6}$$

where $X_{\rm MSB}$, $X_{\rm ISB}$, and $X_{\rm LSB}$ correspond to the most significant, intermediate, and least significant bits, respectively, and

$$N = N_{\rm MSB} + N_{\rm ISB} + N_{\rm LSB}. \tag{7}$$

In the remainder of the paper, we will consider the merits of the bus-splitting architectures in Figs. 3(b)–(d) compared to the architecture in Fig. 3(a). We will show when and how they can be used to achieve similar spectral performance but using less area and power. First we consider a pseudorandom input resulting from dither and then a sinusoidal input.

## IV. Dithered EFM

### A. Conventional Dithered EFM

Fig. 4 shows a simplified block diagram of the dithered third-order EFM (EFM3) that we consider in this work. In this scheme, a 1-bit dither sequence, $d$, low-pass filtered by a shaping filter $V(z) = (1-z^{-1})^R$, is added to the signal, $s$, giving

$$x = s + v * d \tag{8}$$

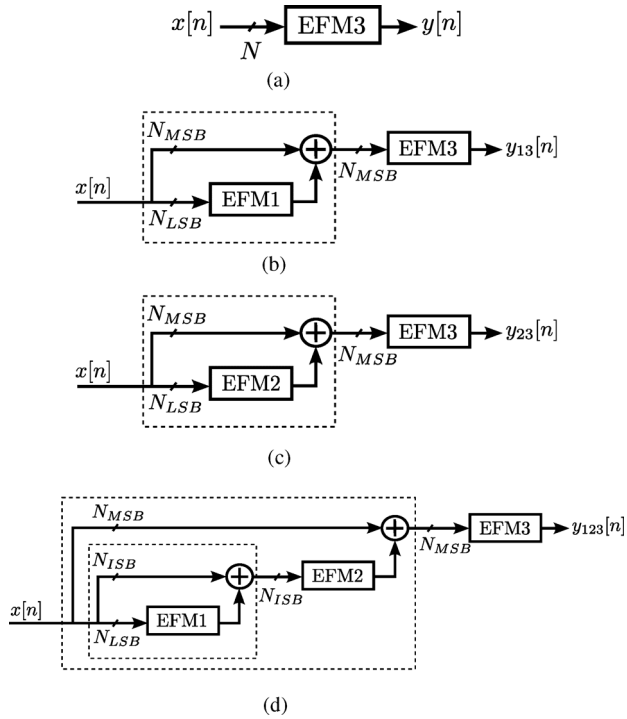


Fig. 3. Block diagrams of the conventional and bus-splitting EFM architectures. (a) Conventional architecture, (b) Bus-splitting 1-3 EFM3, (c) Bus-splitting 2-3 EFM3, (d) Nested bus-splitting 1-2-3 EFM3.

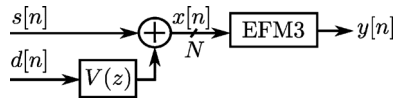


Fig. 4. Block diagram of a dithered EFM3.

where "*" denotes the convolution operator. It has been proven that the EFM quantization noise is white, uniformly distributed and independent of the DDSM input if $R \leq L-2$, where $L$ is the order of the DDSM [6]; this ensures a spur-free output spectrum. Consequently, in the case of third-order lowpass DDSMs, both non-shaped $(R=0)$ and first-order shaped $(R=1)$ dither can be used to suppress spurious tones.

The minimum cycle length of a dithered DDSM is usually very large. Consequently, the tone spacing is typically very small and the discrete output spectrum tends toward a continuous spectrum. Assuming white quantization noise, the noise at the output can be estimated using the traditional linear model [18]

$$\mathcal{L}(f) = \frac{\Delta^2}{12} |{\rm NTF}(z)|^2_{z=e^{j2\pi f/f_s}} \tag{9}$$

where $\Delta$ is the quantization interval, ${\rm NTF}(z)$ is the noise transfer function which shapes the quantization noise and $f_s$ is the (uniform) sampling frequency.

### B. Dithered Bus-Splitting DDSM

Consider the dithered bus-splitting architectures shown in Figs. 5(a) and (b). We present the design methodology for the dithered nested bus-splitting 1-2-3 EFM3 in detail and present

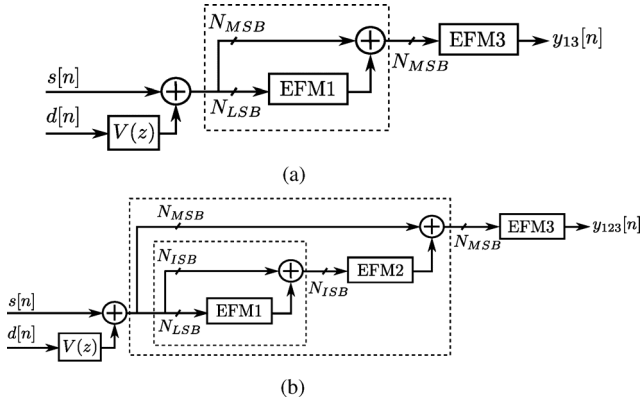


Fig. 5. The dithered bus-splitting 1-3 EFM3 (a) and the dithered nested bus-splitting 1-2-3 EFM3 (b). (a) Dithered bus-splitting 1-3 EFM3, (b) Dithered nested bus-splitting 1-2-3 EFM3.

a design equation for the bus-splitting 1-3 EFM3. The output of the nested bus-splitting 1-2-3 EFM3 can be written as [1]

$$Y_{123}(z) = \frac{X(z)}{2^N} + N_1(z) + N_2(z) + N_3(z) \tag{10}$$

where $N_1(z) = (1 - z^{-1})\epsilon_{Q1b}(z)/(2^{N_{\rm LSB}} \cdot 2^{N_{\rm MSB}+N_{\rm ISB}})$ is the shaped contribution of the quantizer in EFM1, $N_2(z) = (1-z^{-1})^2\epsilon_{Q2}(z)/(2^{N_{\rm ISB}} \cdot 2^{N_{\rm MSB}})$ is the shaped contribution of the quantizer in EFM2 and $N_3(z) = (1-z^{-1})^3 E_{123}(z)/2^{N_{\rm MSB}}$ is the shaped contribution from the quantizer in EFM3. Note that $\epsilon_{Q1b}(z), \epsilon_{Q2}(z)$ and $E_{123}(z)$ are the Z-transforms of the quantization errors of the EFM1, EFM2 and EFM3 in the bus-splitting 1-2-3 architecture, respectively. Using (9), the PSDs of the filtered error signals $N_1, N_2$, and $N_3$ can be approximated by

$$\mathcal{L}_1(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{\rm MSB}+N_{\rm ISB}}}\right)^2 |(1 - z^{-1})|^2_{z=e^{j2\pi f/f_s}} \tag{11}$$

$$\mathcal{L}_2(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{\rm MSB}}}\right)^2 |(1 - z^{-1})^2|^2_{z=e^{j2\pi f/f_s}} \tag{12}$$

$$\mathcal{L}_3(f) = \frac{1}{12}|(1 - z^{-1})^3|^2_{z=e^{j2\pi f/f_s}}. \tag{13}$$

### C. Zeroth-Order Dither

In the case of a DDSM with zeroth-order LSB dithering and a constant input, the low frequency noise floor is determined by the dither signal. In the case of zeroth-order dither, the level of the noise floor is [18]

$$\mathcal{L}_{nf0}(f) = \frac{1}{12}\left(\frac{1}{2^N}\right)^2 \tag{14}$$

and the largest frequency at which the PSD of the dithering is larger than the contribution from the quantization noise of EFM3 in the nested bus-splitting 1-2-3 EFM3 architecture, $e_{123}$, is given by

$$f_0 = \frac{1}{\pi \cdot 2^{N/3}} \cdot \frac{f_s}{2}. \tag{15}$$

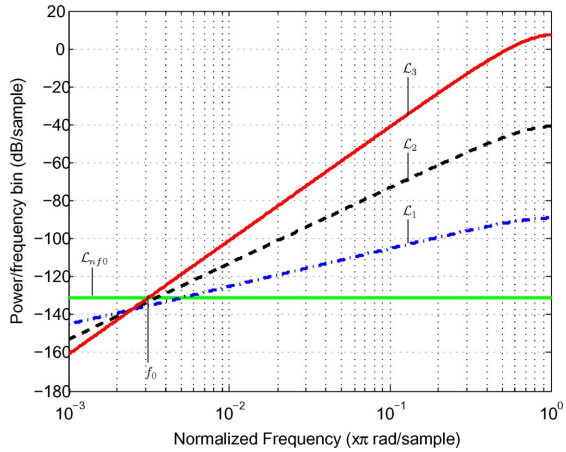


Fig. 6. Masking (dashed-dotted) $\mathcal{L}_1$ and (dashed) $\mathcal{L}_2$ below (solid) $\mathcal{L}_3$ at $f_0$. $\mathcal{L}_1, \mathcal{L}_2, \mathcal{L}_3$ and $\mathcal{L}_{nf0}$ are defined by (11)–(13) and (14). In this example, $N_{\rm LSB} = 6$, $N_{\rm ISB} = 7$, and $N_{\rm MSB} = 7$.

Fig. 6 shows typical contributions $\mathcal{L}_1, \mathcal{L}_2, \mathcal{L}_3$, and $\mathcal{L}_{nf0}$ for a zeroth-order dithered nested bus-splitting 1-2-3 EFM3. The corner frequency $f_0$ is defined by the intersection of $\mathcal{L}_3$ and $\mathcal{L}_{nf0}$. As $\mathcal{L}_1$ and $\mathcal{L}_2$ are first- and second-order shaped, respectively, we require that

$$\mathcal{L}_1(f_0) < \mathcal{L}_3(f_0) \tag{16}$$

$$\mathcal{L}_2(f_0) < \mathcal{L}_3(f_0) \tag{17}$$

in order to mask the quantization errors of the intermediate EFMs below that of the dithering and the error from EFM3.

Assuming a sufficiently large oversampling rate, we can approximate $\mathcal{L}_1, \mathcal{L}_2$, and $\mathcal{L}_3$ at low frequencies by

$$\mathcal{L}_1(f) \approx \frac{1}{12} \cdot \left(\frac{1}{2^{N_{\rm MSB}+N_{\rm ISB}}}\right)^2 \cdot 2^2 \left(\frac{\pi f}{f_s}\right)^2 \tag{18}$$

$$\mathcal{L}_2(f) \approx \frac{1}{12} \cdot \left(\frac{1}{2^{N_{\rm MSB}}}\right)^2 \cdot 2^4 \left(\frac{\pi f}{f_s}\right)^4 \tag{19}$$

$$\mathcal{L}_3(f) \approx \frac{1}{12} \cdot 2^6 \left(\frac{\pi f}{f_s}\right)^6. \tag{20}$$

Substituting (18), (19), and (20) into the constraints (16) and (17), we obtain

$$\frac{1}{2^{2N_{\rm MSB}+2N_{\rm ISB}}} \cdot \frac{1}{12} \cdot \left(\frac{1}{2^{N/3}}\right)^2 < \frac{1}{12} \cdot \left(\frac{1}{2^{N/3}}\right)^6 \tag{21}$$

$$\frac{1}{2^{2N_{\rm MSB}}} \cdot \frac{1}{12} \cdot \left(\frac{1}{2^{N/3}}\right)^4 < \frac{1}{12} \cdot \left(\frac{1}{2^{N/3}}\right)^6 \tag{22}$$

which reduce to

$$N_{\rm MSB} + N_{\rm ISB} > \frac{2N}{3} \tag{23}$$

$$N_{\rm MSB} > \frac{N}{3}. \tag{24}$$

TABLE I
OPTIMIZED WORDLENGTHS FOR BUS-SPLITTING DDSM3 ARCHITECTURES

| Bus-splitting DDSM | Wordlengths | | |
|---|---|---|---|
| | $N_{LSB}$ | $N_{ISB}$ | $N_{MSB}$ |
| (a) 1-3 | $N$-$M$ | - | $M$ |
| (b)1-2-3 | $N$-$M$ | $M$-$L$ | $L$ |

Based on (23) and (24), if the word length $N$ of the input is known, the optimum wordlengths $N_{\rm LSB}, N_{\rm ISB}$, and $N_{\rm MSB}$ of the EFM1, EFM2, and EFM3 can be calculated from

$$N_{\rm MSB} = \left\lceil \frac{N}{3} \right\rceil \tag{25}$$

$$N_{\rm ISB} = \left\lceil \frac{2N}{3} \right\rceil - N_{\rm MSB} \tag{26}$$

$$N_{\rm LSB} = N - N_{\rm MSB} - N_{\rm ISB}. \tag{27}$$

Note that, in contrast to the design methodology for the ditherless DDSM [1], there is no cycle-length criterion to be satisfied and the design methodology for the dithered EFM does not require the wordlength of the first stage of the bus-splitting DDSM architecture to be increased. A similar analysis can be performed to determine the optimum wordlengths for the bus-splitting 1-3 EFM3 with zeroth-order dither.

In order to design a bus-splitting EFM with a PSD which is similar to that of a conventional $N_0$-bit EFM3 with zeroth-order dither, the design procedure is as follows:

- Choose $N = N_0$.
- Choose the desired bus-splitting architecture and determine the optimized wordlengths from Table I using $M = \lceil (2N)/(3) \rceil$ and $L = \lceil (N/3) \rceil$, as appropriate.

### D. First-Order Dither

If first-order shaped dither is applied to the input of the EFM, its noise floor is defined by

$$\mathcal{L}_{nf1}(f) = \frac{1}{12}\left(\frac{1}{2^N}\right)^2 |2\sin(\pi f/f_s)|^2 \tag{28}$$

and the largest frequency at which the PSD of the dithering is larger than the contribution from $e_{123}$ is given by

$$f_1 = \frac{1}{\pi \cdot 2^{N/2}} \cdot \frac{f_s}{2}. \tag{29}$$

Fig. 7 shows typical contributions $\mathcal{L}_2, \mathcal{L}_3$, and $\mathcal{L}_{nf1}$ for a first-order dithered nested bus-splitting 1-2-3 EFM3. The corner frequency in this case, $f_1$, is defined by the intersection of $\mathcal{L}_3$ and $\mathcal{L}_{nf1}$. Note that we have not shown $\mathcal{L}_1$ in Fig. 7. Since $\mathcal{L}_1$ is first-order shaped, we require that $\mathcal{L}_1 < \mathcal{L}_{nf1}$, which can be expressed as

$$\frac{1}{12}\cdot\frac{1}{2^{2N_{\rm MSB}+2N_{\rm ISB}}}\cdot 2^2(\pi f/f_s)^2 \le \frac{1}{12}\frac{1}{2^{2N}}\cdot 2^2(\pi f/f_s)^2. \tag{30}$$

This in turn reduces to

$$N_{\rm MSB} + N_{\rm ISB} \ge N. \tag{31}$$

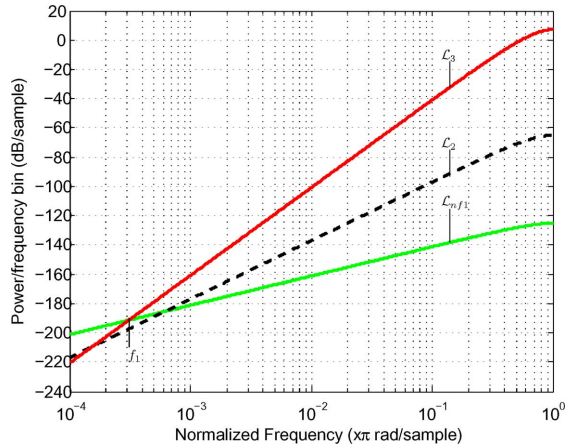


Fig. 7. Masking (dashed) $\mathcal{L}_2$ below (solid) $\mathcal{L}_3$ at $f_1$. $\mathcal{L}_2, \mathcal{L}_3$ and $\mathcal{L}_{nf1}$ are defined by (12), (13) and (28). In this example, $N_{\rm LSB} = 0, N_{\rm ISB} = 9$, and $N_{\rm MSB} = 11$.

Since our objective is to *minimize* the overall hardware requirement, we choose $N_{\rm MSB} + N_{\rm ISB} = N$. Recall that $N_{\rm MSB} + N_{\rm ISB} + N_{\rm LSB} = N$ by definition; hence $N_{\rm LSB} = 0$. Thus, (31) implies that it is not necessary to use a first-order EFM to shape the $N_{\rm LSB}$ bits of the input word. In this case, the nested bus-splitting 1-2-3 EFM3 in Fig. 3(d) reduces to the bus-splitting 2-3 EFM3 in Fig. 3(c).

Next, $\mathcal{L}_2$ needs to be masked by $\mathcal{L}_3$, as shown schematically in Fig. 7. Thus, the word-length strategy for the DDSM2 requires that

$$\mathcal{L}_2(f_1) < \mathcal{L}_3(f_1) \tag{32}$$

This can be expressed as

$$\frac{1}{2^{2N_{\rm MSB}}}\cdot\frac{1}{12}\cdot\left(\frac{1}{2^{N/2}}\right)^4 < \frac{1}{12}\cdot\left(\frac{1}{2^{N/2}}\right)^6 \tag{33}$$

which gives

$$N_{\rm MSB} > \frac{N}{2}. \tag{34}$$

In order to design a bus-splitting 2-3 EFM3 with a PSD similar to that of a conventional $N_0$-bit EFM3 with first-order dither, the design procedure is as follows:

- Choose $N = N_0$.
- Choose $N_{\rm MSB} = \lceil N/2 \rceil$.
- Choose $N_{\rm ISB} = N - N_{\rm MSB}$.

### E. Design Examples

In this subsection, we present a design example for a zeroth-order dithered 20-bit EFM3. Applying design equations (25)–(27), the appropriate wordlengths for the nested bus-splitting 1-2-3 EFM3 are $N_{\rm MSB} = 7, N_{\rm ISB} = 7$, and $N_{\rm LSB} = 6$. A 7-7-6-bit nested bus-splitting 1-2-3 EFM3 is simulated to show typical contributions $N_1, N_2$, and $N_3$ (see Figs. 8–10)[1].

[1]A Hanning window with $2^{20}$ output samples was used when computing the spectra in this section based on the periodogram method described in [19].

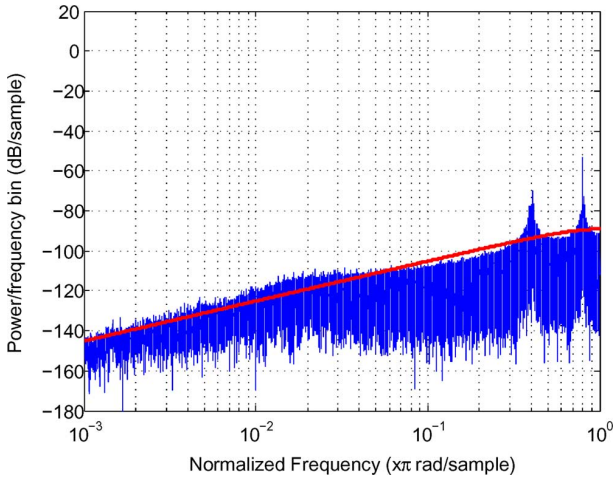


Fig. 8. Simulated PSD for $N_1$ when $N_{\mathrm{MSB}} = 7$, $N_{\mathrm{ISB}} = 7$, and $N_{\mathrm{LSB}} = 6$; the input is 104857. The smooth curve is $\mathcal{L}_1$ (11).

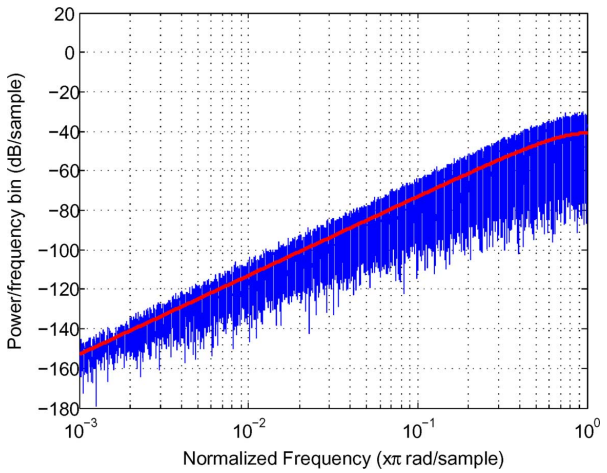


Fig. 9. Simulated PSD for $N_2$ when $N_{\mathrm{MSB}} = 7$, $N_{\mathrm{ISB}} = 7$, and $N_{\mathrm{LSB}} = 6$; the input is 104857. The smooth curve is $\mathcal{L}_2$ (12).

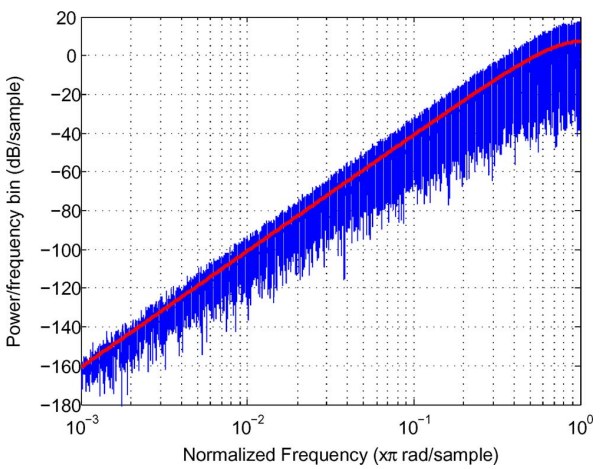


Fig. 10. Simulated PSD for $N_3$ when $N_{\mathrm{MSB}} = 7$, $N_{\mathrm{ISB}} = 7$, and $N_{\mathrm{LSB}} = 6$; the input is 104857. The smooth curve is $\mathcal{L}_3$ (13).

Note that, in the case of Fig. 8, the simulated $N_1$ curve is not well approximated by the theoretical $\mathcal{L}_1$ curve at high frequencies. This is not surprising given the fact that it has been established that LSB dither cannot make the quantization noise in a first-order DDSM white [5]. In the case of non-white quantization noise, the exact shape of the DDSM output spectrum is difficult to predict. To the best of the authors' knowledge, this problem has not been addressed satisfactorily in the literature. In any case, there is good matching at low frequencies which is the most important region for the design methodology, given that the contribution at high frequencies is masked by the higher order shaped terms.

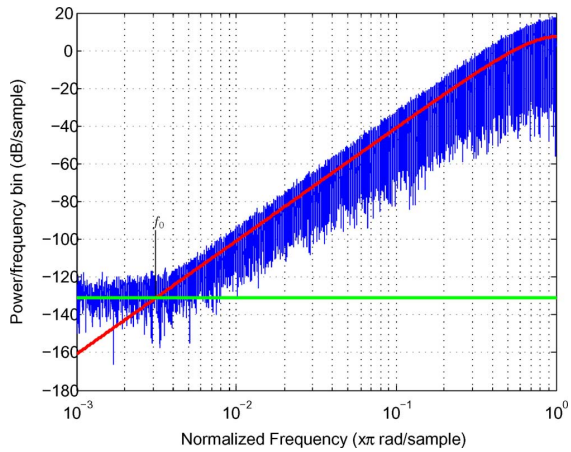


Fig. 11. Simulated PSD at the output of a zeroth-order dithered 20-bit EFM3; the input is 104857. The smooth curves are $\mathcal{L}_3$ (13) and $\mathcal{L}_{nf0}$ (14).

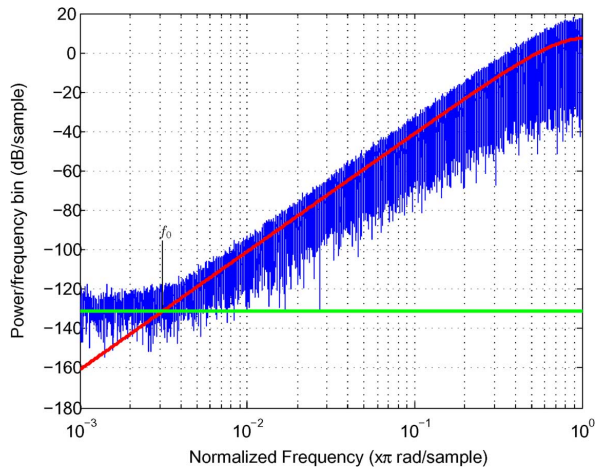


Fig. 12. Simulated PSD at the output of a zeroth-order dithered 7-7-6-bit nested bus-splitting 1-2-3 EFM3; the input is 104857. The smooth curves are $\mathcal{L}_3$ (13) and $\mathcal{L}_{nf0}$ (14).

The simulated PSD for a conventional zeroth-order dithered 20-bit EFM3 is shown in Fig. 11. The PSD of the 7-7-6-bit nested bus-splitting 1-2-3 EFM3 is shown in Fig. 12. Note that the $N_1$ and $N_2$ components lie below the spectral envelope of $N_3$ above $f_0$ and are therefore masked by it, as expected. Consequently, $N_1$ and $N_2$ do not affect the overall performance of the nested bus-splitting 1-2-3 EFM3.

The hardware requirements for (i) a conventional 20-bit EFM3 and (ii) the 14-6-bit 1-3 EFM3 and 7-7-6-bit 1-2-3 EFM3 architectures with zeroth-order dither are summarized in Table II. Note that the hardware of the dither block has been

TABLE II
HARDWARE AND POWER CONSUMPTION OF A CONVENTIONAL 20-BIT EFM3 AND THE BUS-SPLITTING EFM ARCHITECTURES USING SYNOPSYS DESIGN COMPILER AND PRIMETIME [20]

| EFM | area ($\mu m^2$) | power ($\mu W$) | slack (ns) |
|---|---|---|---|
| (a) 20-bit EFM3 | 1388.2 | 162.7 | 6.78 |
| (b) 14-6-bit 1-3 EFM3 | 1083.2 | 125.7 | 7.36 |
| ((b)/(a))% | 78 | 77 | 108 |
| (c) 7-7-6-bit 1-2-3 EFM3 | 885.6 | 98 | 7.36 |
| ((c)/(a))% | 64 | 60 | 108 |
| (d) 11-9-bit 2-3 EFM3 | 1158.1 | 124.4 | 7.23 |
| ((d)/(a))% | 83 | 76 | 107 |

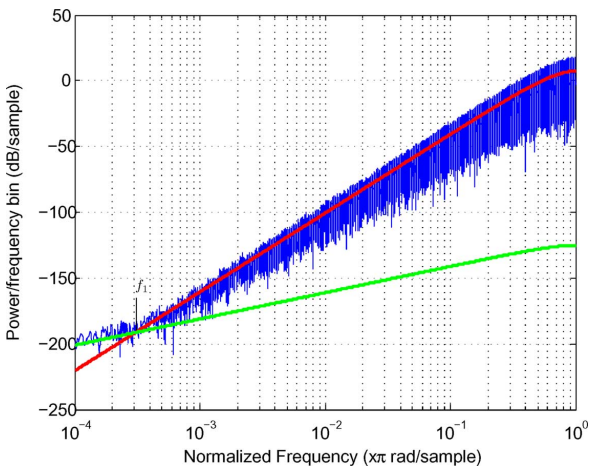


Fig. 13. Simulated PSD at the output of a first-order dithered 20-bit EFM3; the input is 3277. The smooth curves are $\mathcal{L}_3$ (13) and $\mathcal{L}_{nf1}$ (28).

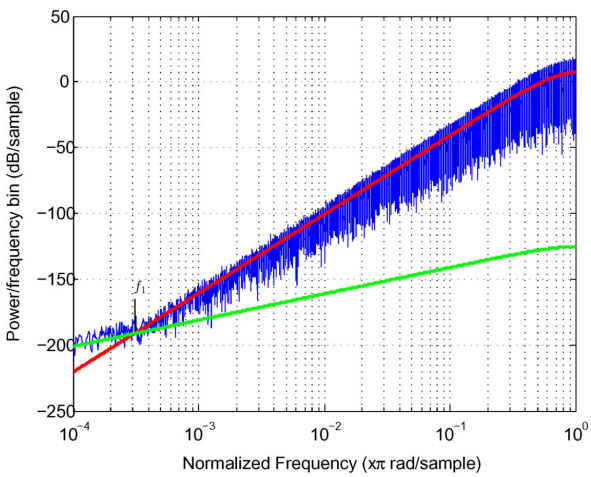


Fig. 14. Simulated PSD at the output of a first-order dithered 11-9-bit bus-splitting 2-3 EFM3; the input is 3277. The smooth curves are $\mathcal{L}_3$ (13) and $\mathcal{L}_{nf1}$ (28).

excluded in order to allow a direct comparison of the relative hardware consumption (RHC) of the nested architectures.

The simulated PSD for a conventional 20-bit EFM3 with first-order shaped additive input dither is shown in Fig. 13. Applying the design equation (34), the wordlengths of the bus-splitting 2-3 EFM3 are $N_{\mathrm{MSB}} = 11$ and $N_{\mathrm{ISB}} = 9$. The simulated PSD for the 11-9-bit bus-splitting 2-3 EFM3 is shown in Fig. 14. As expected, the bus-splitting EFM3 achieves an almost identical PSD compared to the conventional 20-bit EFM3.

The hardware requirements for the bus-splitting 2-3 EFM3 architecture with first-order dither are also summarized in Table II. Note that the nested bus-splitting 7-7-6-bit 1-2-3 EFM3 requires 36% less area and 40% less power than the equivalent 20-bit EFM3. Note also that the 14-6-bit bus splitting 1-3 EFM3 consumes more power than the 11-9-bit bus-splitting 2-3 EFM3 while consuming less area, indicating a higher level of switching activity in the bus-splitting 1-3 EFM3 architecture. The slack value is higher for the 14-6-bit bus-splitting 1-3 EFM3, suggesting that a portion of its extra power is being used to allow higher operation speed.

## V. DDSM WITH SINUSOIDAL INPUT

In this section, we will discuss the merits of bus-splitting in the case of sinusoidal inputs. Using the concept of error masking [18], we have developed a design methodology which rigorously quantifies the effects of the various parameters on the effective-number of bits (ENOB) at the output for bus-splitting DDSMs with sinusoidal inputs.

### A. Oversampled Quantized Sinusoid

Consider a signal $x$ with bandwidth $f_B$ that is sampled at a frequency $f_s$ and then quantized using an $N$-bit quantizer with a quantization step $\Delta$. Assuming a full-scale sinusoidal input, the powers of the signal and quantization noise in the signal band of interest are given by [21]

$$P_{\sin} = \frac{(\Delta \cdot 2^N)^2}{8} \tag{35}$$

$$P_Q = \frac{\Delta^2}{12 \cdot \mathrm{OSR}} \tag{36}$$

respectively, where the oversampling ratio is defined by $\mathrm{OSR} = (f_s)/(2f_B)$. The SNR is defined by

$$\mathrm{SNR} = \frac{P_{\sin}}{P_Q}. \tag{37}$$

Substituting (35) and (36) into (37) gives

$$\mathrm{SNR} = 2^{2N}\left(\frac{12}{8}\right)\mathrm{OSR}. \tag{38}$$

The corresponding SNR in dB is given by

$$\mathrm{SNR}_{dB} = 6.02N + 1.76 + 3.01\log_2 \mathrm{OSR}. \tag{39}$$

The ENOB is defined by

$$\mathrm{ENOB} = \frac{\mathrm{SNR}_{dB} - 1.76}{6.02}. \tag{40}$$

Substituting (39) into (40) gives

$$\mathrm{ENOB} = N + 0.5\log_2 \mathrm{OSR}. \tag{41}$$

### B. Oversampled Quantized Sinusoid Applied to an EFM Alone

Next, consider a signal $x$ with bandwidth $f_B$ that is sampled at a frequency $f_s$ and then quantized using an $N$-bit quantizer with a quantization step $\Delta$, to produce an output $x_B$. Assume that the signal $x_B$ is applied to an $l$th order EFM with additive

white quantization noise $e$ and $\mathrm{NTF}(z) = (1 - z^{-1})^l$. The output of the EFM can be written in the z-domain as

$$Y(z) = \frac{1}{2^N} X_B(z) + \frac{1}{2^N}(1 - z^{-1})^l E(z) \tag{42}$$

In this case, the total power of the in-band quantization noise is given by [11]

$$\begin{aligned} q_{\mathrm{rms}}^2 &= \int_0^{f_B} \frac{1}{2^{2N}}(1 - e^{-j2\pi f/f_s})^{2l} e_{\mathrm{rms}}^2 \, df \\ &= \frac{1}{12} \cdot \frac{\pi^{2l}}{(2l+1)\mathrm{OSR}^{2l+1}} \end{aligned} \tag{43}$$

where we have assumed that $e_{\mathrm{rms}}^2 = \Delta_Q^2/12$. Note that the step size of the quantizer in the $l$th order EFM is given by $\Delta_Q = 2^N$. Typically, $\mathrm{STF}(z)$ is an all-pass filter or a delay. Consequently, the SNR at the output of the EFM$l$ is given by

$$\begin{aligned} \mathrm{SNR} &= \frac{\frac{\Delta^2}{8}}{\frac{\Delta^2}{2^{2N} \cdot 12 \cdot \mathrm{OSR}} + \frac{1}{12}\left(\frac{\pi^{2l}}{2l+1}\right)\left(\frac{1}{\mathrm{OSR}}\right)^{2l+1}} \\ &= \frac{2^{2N}\left(\frac{12}{8}\right)\mathrm{OSR}}{1 + \left(\frac{2^{2N}}{2l+1}\right)\left(\frac{\pi}{\mathrm{OSR}}\right)^{2l}} \end{aligned} \tag{44}$$

where we have assumed that $\Delta = 1$ which corresponds to the least significant bit of a digital implementation. Comparing (38) and (44), the degradation in the SNR caused by passing the quantized signal through an $l$th order low-pass EFM is given by

$$\Delta\mathrm{SNR}_{dB} = 10\log_{10}\left(1 + \left(\frac{2^{2N}}{2l+1}\right)\left(\frac{\pi}{\mathrm{OSR}}\right)^{2l}\right). \tag{45}$$

In the case of a DDSM with a quantized sinusoidal input, the level of the noise floor in the output PSD at low frequencies is determined by the number of bits of the sinusoid. The output also contains a component due to the quantization noise of the DDSM. This is illustrated in Fig. 15 which shows the output PSD of a conventional EFM3 with $\mathrm{OSR} = 32$, $f_B = 20$ kHz and $N = 16$. Note that, in this case, the simulated ENOB value obtained using the technique described in [22] with a Hanning window of $2^{20}$ terms is 13.94, and is dominated by the rising quantization noise introduced by the EFM3 beginning at approximately 5 kHz

In order to maximize the ENOB while simultaneously minimising the OSR required for a given value of $N$ and $f_B$, one must determine the corner frequency, $f_0$, at which the PSD of the noise floor and shaped quantization noise intersect. This can be calculated as

$$\frac{1}{12}|2\sin(\pi f_0/f_s)|^{2l} = \frac{1}{12 \cdot 2^{2N}}. \tag{46}$$

Assuming

$$\sin(\pi f_0/f_s) \approx \pi f_0/f_s \quad \text{for } f_0 \ll f_s \tag{47}$$

this gives

$$f_0 = \frac{1}{\pi \cdot 2^{N/l}} \cdot \frac{f_s}{2}. \tag{48}$$

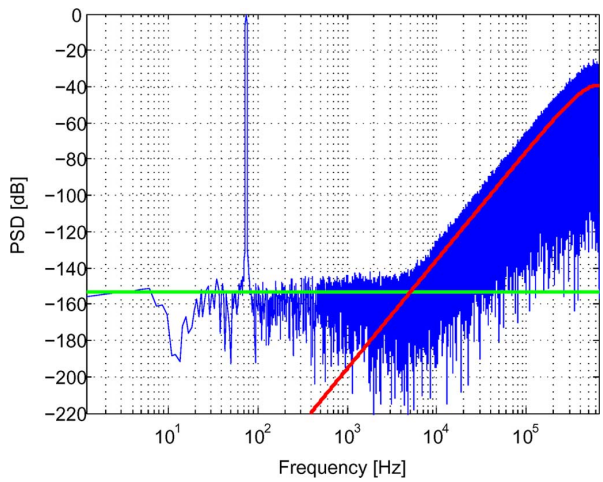


Fig. 15. PSD of the output of the conventional EFM3 with $\mathrm{OSR} = 32$, $f_B = 20$ kHz and $N = 16$. The simulated $\mathrm{ENOB} = 13.94$. The theoretical $\mathrm{ENOB} = 13.96$. The solid curves show the contributions of the quantized sinusoid and EFM3 given by (14) and (20), respectively.

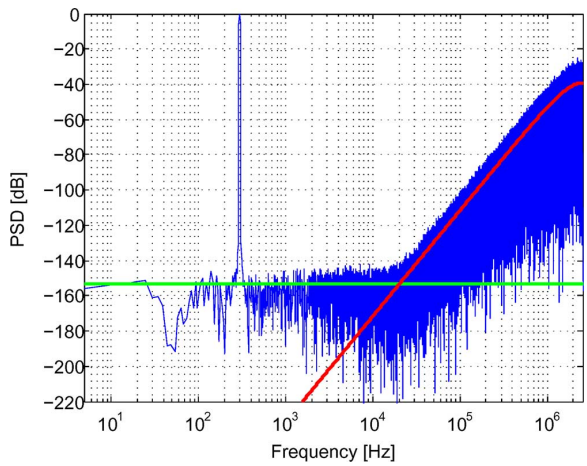


Fig. 16. PSD of the output of the conventional EFM3 with $\mathrm{OSR} = 128$, $f_B = 20$ kHz and $N = 16$. The simulated $\mathrm{ENOB} = 19.54$. The theoretical $\mathrm{ENOB} = 19.41$. The solid curves show the contributions of the quantized sinusoid and EFM3 given by (14) and (20), respectively.

Setting $f_0 = f_B$ yields

$$\mathrm{OSR} = 2^{N/l}\pi. \tag{49}$$

Using (49) with $N = 16$ and $l = 3$ yields a minimum value of $\mathrm{OSR} \approx 127$. Fig. 16 which shows the output PSD of a conventional EFM3 with $\mathrm{OSR} = 128$, $f_B = 20$ kHz and $N = 16$. In this case, the simulated ENOB is 19.54.

### C. Oversampled Quantized Sinusoid With Bus-Splitting Alone

We consider again a signal $x$ with bandwidth $f_B$ that has been sampled at frequency $f_s$ and quantized by an $N$-bit quantizer, producing an output $x_B$. This time, the $N$-bit word $x_B$ is split so that the lower $N_{\mathrm{LSB}}$ bits are first applied to an $l$th order DDSM, as shown in Fig. 17. The output of this DDSM is combined with

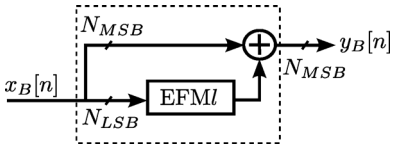


Fig. 17. A quantized input signal $x_B$ is split such that the lower $N_{\rm LSB}$ bits are applied to an $l$th-order DDSM before being recombined with the upper $N_{\rm MSB}$ bits.

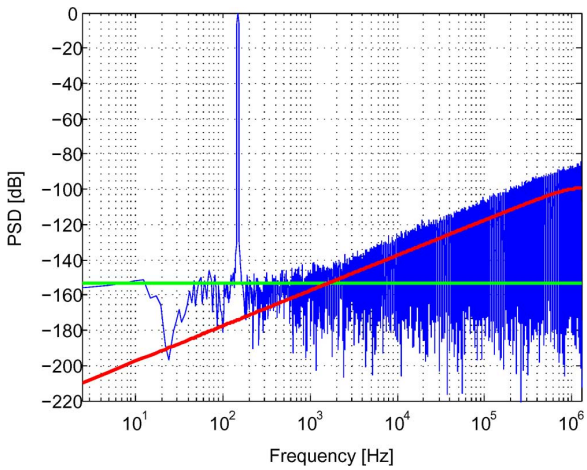


Fig. 18. PSD of a full-scale sinusoid with 20 kHz bandwidth quantized to 16 bits with $OSR = 64$ using the scheme of Fig. 17 with $N_{\rm MSB} = 8$ and $N_{\rm LSB} = 8$ for the case $l = 1$. The simulated $\rm ENOB = 15.92$. The theoretical $\rm ENOB = 16.14$. The solid curves show the contributions of the quantized sinusoid and EFM1, respectively.

the upper $N_{\rm MSB}$ bits to form an $N_{\rm MSB}$-bit word. Using (44), we can write the SNR of $y_B$ as

$$\mathrm{SNR} = \frac{2^{2N}\left(\frac{12}{8}\right)\mathrm{OSR}}{1+\left(\frac{2^{2N_{\rm LSB}}}{2l+1}\right)\left(\frac{\pi}{\mathrm{OSR}}\right)^{2l}} \tag{50}$$

Comparing (50) with (38), if

$$\left(\frac{2^{2N_{\rm LSB}}}{2l+1}\right)\left(\frac{\pi}{\mathrm{OSR}}\right)^{2l} \ll 1 \tag{51}$$

then the bus-splitting DDSM does not significantly degrade the SNR.

This idea is illustrated graphically in Figs. 18 and 19, which show the simulated PSDs of a 16-bit full-scale sinusoid with 20 kHz bandwidth using the scheme of Fig. 17 for two different cases; (a) $l = 1$ and (b) $l = 2$.

The digital word is split such that the lower 8 bits are applied to a low-order EFM and the output is combined with the upper 8-bits. The simulated ENOB values for cases (a) and (b) are 15.92 and 19.07, respectively. Note, using (41), that $\rm ENOB = 19.0$ for the original quantized sinusoid. Depending on the choice of $l$ and the partitioning of the input word, a reduction in the wordlength of the sinusoid can be achieved with or without significantly degrading the quality of the output. For the above parameters, using $l = 1$ results in a reduction in the ENOB by 3 bits but the reduction is negligible when $l = 2$.

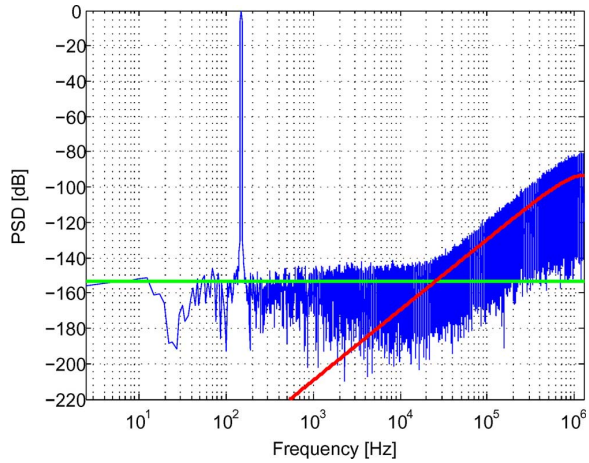


Fig. 19. PSD of a full-scale sinusoid with 20 kHz bandwidth quantized to 16 bits with $\rm OSR = 64$ using the scheme of Fig. 17 with $N_{\rm MSB} = 8$ and $N_{\rm LSB} = 8$ for the case $l = 2$. The simulated $\rm ENOB = 19.07$. The theoretical $\rm ENOB = 18.96$. The solid curves show the contributions of the quantized sinusoid and EFM2, respectively.

### *D. Oversampled Quantized Sinusoid Applied to a Bus-Splitting EFM*

We can estimate the SNRs at the outputs of the bus-splitting EFM architectures in Figs. 3(b)–(d) and compare them with the conventional case in Fig. 3(a). The SNR at the output of the conventional EFM3 is

$$\mathrm{SNR}_3 = \frac{\frac{\Delta^2}{8}}{\mathcal{N}_0 + \mathcal{N}_3} \tag{52}$$

where $\mathcal{N}_0$ and $\mathcal{N}_3$ are the quantization noise terms associated with the sinusoid and EFM3; these are defined by

$$\mathcal{N}_0 = \frac{1}{12}\left(\frac{1}{2^{N_{\rm MSB}+N_{\rm LSB}}}\right)^2 \frac{1}{\mathrm{OSR}} \tag{53}$$

and

$$\mathcal{N}_3 = \frac{1}{12}\frac{\pi^6}{7\mathrm{OSR}^7} \tag{54}$$

respectively. The SNR at the output of the bus-splitting 1-3 EFM3 shown in Fig. 3(b) is

$$\mathrm{SNR}_{13} = \frac{\frac{\Delta^2}{8}}{\mathcal{N}_0 + \mathcal{N}_1 + \mathcal{N}_3} \tag{55}$$

where

$$\mathcal{N}_1 = \frac{1}{12}\left(\frac{1}{2^{N_{\rm MSB}}}\right)^2 \frac{\pi^2}{3\mathrm{OSR}^3} \tag{56}$$

and $\mathcal{N}_0$ and $\mathcal{N}_3$ are defined by (53) and (54). The reduction in the SNR is defined by $\Delta\mathrm{SNR}_{13} = \mathrm{SNR}_3 - \mathrm{SNR}_{13}$. On a log scale,

$$\Delta\mathrm{SNR}_{13}\ \mathrm{dB} = 10\log\left(\frac{\mathcal{N}_0 + \mathcal{N}_1 + \mathcal{N}_3}{\mathcal{N}_0 + \mathcal{N}_3}\right). \tag{57}$$

The corresponding reduction in ENOB is defined by

$$\begin{aligned}\Delta\mathrm{ENOB}_{13} &= \frac{10}{6.02}\log\left(\frac{\mathcal{N}_0 + \mathcal{N}_1 + \mathcal{N}_3}{\mathcal{N}_0 + \mathcal{N}_3}\right) \\ &= \frac{10}{6.02}\log\left(1 + \frac{\mathcal{N}_1}{\mathcal{N}_0 + \mathcal{N}_3}\right)\end{aligned} \tag{58}$$

The SNR at the output of a nested bus-splitting 1-2-3 EFM3 is

$$\mathrm{SNR}_{13} = \frac{\frac{\Delta^2}{8}}{\mathcal{N}_0 + \mathcal{N}_1 + \mathcal{N}_2 + \mathcal{N}_3} \tag{59}$$

where

$$\mathcal{N}_0 = \frac{1}{12}\left(\frac{1}{2^{N_{\mathrm{MSB}}+N_{\mathrm{ISB}}+N_{\mathrm{LSB}}}}\right)^2 \frac{1}{\mathrm{OSR}} \tag{60}$$

$$\mathcal{N}_1 = \frac{1}{12}\left(\frac{1}{2^{N_{\mathrm{MSB}}+N_{\mathrm{ISB}}}}\right)^2 \frac{\pi^2}{3\mathrm{OSR}^3} \tag{61}$$

$$\mathcal{N}_2 = \frac{1}{12}\left(\frac{1}{2^{N_{\mathrm{MSB}}}}\right)^2 \frac{\pi^4}{5\mathrm{OSR}^5} \tag{62}$$

$$\mathcal{N}_3 = \frac{1}{12}\frac{\pi^6}{7\mathrm{OSR}^7}. \tag{63}$$

The reduction in the SNR is defined by $\Delta\mathrm{SNR}_{123} = \mathrm{SNR}_3 - \mathrm{SNR}_{123}$. On a log scale,

$$\Delta\mathrm{SNR}_{123}\ \mathrm{dB} = 10\log\left(\frac{\mathcal{N}_0 + \mathcal{N}_1 + \mathcal{N}_2 + \mathcal{N}_3}{\mathcal{N}_0 + \mathcal{N}_3}\right). \tag{64}$$

The corresponding reduction in ENOB is defined by

$$\Delta\mathrm{ENOB}_{123} = \frac{10}{6.02}\log\left(1 + \frac{\mathcal{N}_1 + \mathcal{N}_2}{\mathcal{N}_0 + \mathcal{N}_3}\right). \tag{65}$$

### *E. Design Methodology*

Using the hardware estimation technique presented in [1], we can estimate the RHC of the of the bus-splitting 1-3 EFM3 as

$$\mathrm{RHC}_{13} \approx \frac{18N_{\mathrm{LSB}} + 72N_{\mathrm{MSB}} + 120}{72N + 20} \times 100\%. \tag{66}$$

By adjusting the wordlengths $N_{\mathrm{MSB}}$ and $N_{\mathrm{LSB}}$, we can keep $\Delta\mathrm{ENOB}_{13}$ less than a prescribed value using (58) while minimising the required hardware using (66). We present a design example for a conventional 16-bit EFM3 with $\mathrm{OSR} = 128$. Using (58), a specification of $\Delta\mathrm{ENOB}_{13} \leq 0.5$ corresponds to

$$\frac{\mathcal{N}_1}{\mathcal{N}_0 + \mathcal{N}_3} \leq 1. \tag{67}$$

Substituting (53), (54), and (56) into (67) and solving to minimise (66) yields $N_{\mathrm{MSB}} = 10$ and $N_{\mathrm{LSB}} = 6$. The PSDs of the conventional 16-bit EFM3 and 10-6-bit bus-splitting 1-3 EFM3 are shown in Figs. 15 and 20, respectively. The predicted $\Delta\mathrm{ENOB}_{13}$ using (58) is 0.39; the simulated $\Delta\mathrm{ENOB}_{13}$ is 0.48.

The RHC of the nested bus-splitting 1-2-3 EFM3 can be estimated as

$$\mathrm{RHC}_{123} \approx \frac{18N_{\mathrm{LSB}} + 36N_{\mathrm{ISB}} + 72N_{\mathrm{MSB}} + 134}{72N + 20} \times 100\%. \tag{68}$$

Adjusting the wordlengths $N_{\mathrm{MSB}}$, $N_{\mathrm{ISB}}$ and $N_{\mathrm{LSB}}$, we can keep $\Delta\mathrm{ENOB}_{123}$ less than a prescribed value using (65) while minimising the required hardware using (68). Using (65), a specification of $\Delta\mathrm{ENOB}_{123} \leq 0.5$ corresponds to

$$\frac{\mathcal{N}_1 + \mathcal{N}_2}{\mathcal{N}_0 + \mathcal{N}_3} \leq 1. \tag{69}$$

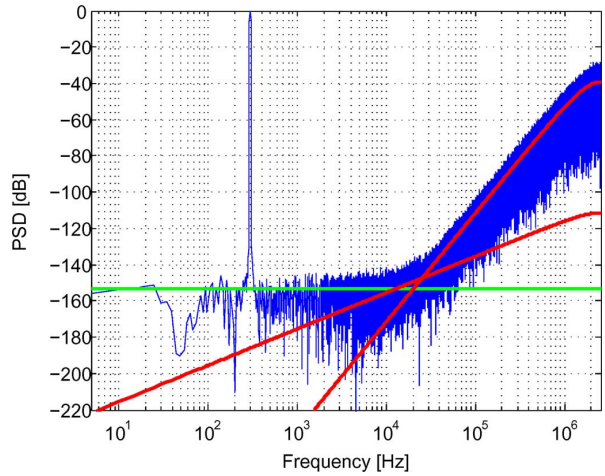


Fig. 20. PSD of the output of the bus-splitting 1-3 EFM3 with $\mathrm{OSR} = 128$, $N_{\mathrm{MSB}} = 10$ and $N_{\mathrm{LSB}} = 6$. The simulated $\mathrm{ENOB} = 19.06$. The theoretical $\mathrm{ENOB} = 19.02$. The solid curves show the contributions of the quantized sinusoid, EFM1 and EFM3 given by (14), (18), and (20), respectively.

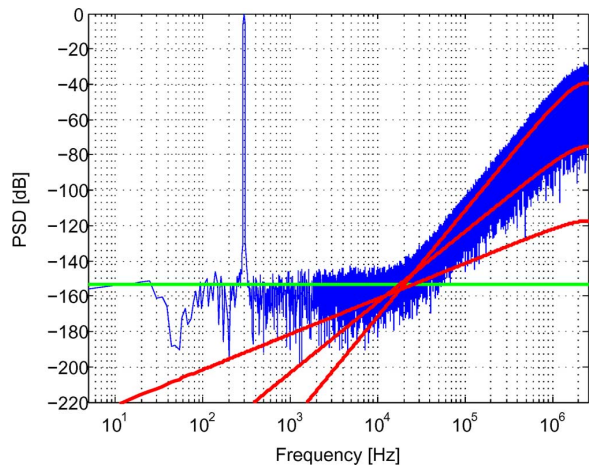


Fig. 21. PSD of the output of the nested bus-splitting 1-2-3 EFM3 with $\mathrm{OSR} = 128$, $N_{\mathrm{MSB}} = 5$, $N_{\mathrm{ISB}} = 6$ and $N_{\mathrm{LSB}} = 5$. The simulated $\mathrm{ENOB} = 19.22$. The theoretical $\mathrm{ENOB} = 19.14$. The solid curves show the contributions of the quantized sinusoid, EFM1, EFM2 and EFM3 given by (14), (18), (19) and (20), respectively.

Substituting (60)–(63) into (69) and solving to minimise (68) yields $N_{\mathrm{MSB}} = 5$, $N_{\mathrm{ISB}} = 6$ and $N_{\mathrm{LSB}} = 5$. The PSD of the output of the 5-6-5-bit nested bus-splitting 1-2-3 EFM3 with $\mathrm{OSR} = 128$ is shown in Fig. 21. The predicted $\Delta\mathrm{ENOB}_{123}$ using (65) is 0.27; the simulated $\Delta\mathrm{ENOB}_{123}$ is 0.32.

The hardware requirements for (i) a conventional 16-bit EFM3 (Fig. 3(a)) and (ii) the bus-splitting EFM architectures (Figs. 3(b), (d)) are summarized in Table III. Note that the nested bus-splitting 1-2-3 EFM3 requires 39% less area and 49% less power than the conventional solution.

## VI. Conclusion

In Part I, we considered a DDSM with a constant input. Such systems have applications in fractional-N frequency synthesizers for generating fixed frequencies. The error masking

TABLE III
HARDWARE AND POWER CONSUMPTION OF THE CONVENTIONAL 16-BIT EFM3 AND THE BUS-SPLITTING EFM ARCHITECTURES USING SYNOPSYS DESIGN COMPILER AND PRIMETIME [20]

| EFM | area ($\mu m^2$) | power ($\mu W$) | slack (ns) |
|---|---|---|---|
| (a) 16-bit EFM3 | 1110.2 | 129.5 | 7.17 |
| (b) 10-6-bit 1-3 EFM3 | 805.3 | 85.5 | 7.74 |
| ((b)/(a))% | 72.5 | 66 | 107.9 |
| (c) 5-6-5-bit 1-2-3 EFM3 | 685.8 | 66.6 | 7.74 |
| ((c)/(a))% | 61.7 | 51.4 | 107.9 |

strategies described in Part I exploit knowledge of the positions of the tones in the undithered case when the input is constant.

In many applications, such as oversampled DACs and synthesizers with in-loop modulation, the input to the DDSM is not constant. In Part II, we have assumed that the input is varying. In this case, the error masking strategy to be adopted exploits knowledge of the shape of the noise floor since the positions of individual tones are typically unknown. Savings in area and power of approximately 40% are possible with minimal degradation of the spectral performance of the modulator.

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