DESIGN-FOR-TEST STRATEGIES FOR ANALOGUE AND MIXED-SIGNAL INTEGRATED CIRCUITS

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Abstract

Recent advances in technology are leading to increases in the complexity and applications of analogue and mixed-signal integrated circuits. This trend has been accomponied by an increase in the complexity of associated test specifications. Furthermore, the use of functional & specification based test programs for the analogue circuitry is being questioned due to high implementation costs, the difficulties associated with quantifying the effectivness of the tests and in many cases difficulties in accessing embedded analogue macros. In addition quality levels expected by integrated circuit (IC) users are increasing, with typical targets currently being better than 40 ppm defect levels. New test solutions are therefore required for these circuit types. Design-for-Test (DfT) strategies are well established for digital circuits, whilst for analogue and mixed signal circuits, few techniques have been proposed and implementation of custom approaches is rare. This paper presents a summary of a number of possible approaches for improving test access by increasing both controllability and observability of internal functional blocks in analogue and mixed-signal ICs, evaluating both their effectiveness and their impact on circuit performance.

1: Introduction

The development of CMOS technology has been driven mainly by digital electronics. Now the trend towards integration of complete systems on single silicon requires mixed analogue-digital technology to realise both digital signal processing and analogue interface functions. This trend creates new problems and requires considerable resources to be applied to the development of new design concepts.

Methodologies for digital Design-for-Test (DfT) are well established and include techniques such as scan path,

boundary scan, and BILBO that have become widely used by industry [1].

On the other hand, it is well known that analogue design is still far from the automation level achieved in the digital design domain. Design of analogue blocks is often the bottleneck in the development of mixed analogue-digital systems. While the analogue section is usually limited to 5 - 10 % of the mixed chip area, its design can take 80 - 90 % of the development time. The trend for test is similar in that there are no formal approaches that can be exploited to minimise test time for analogue functions and no coverage evaluation tools available.

The importance of mixed-signal system development is motivating the development of (DfT) techniques in analogue and mixed signal integrated circuits (ICs), to support increased fault coverage and to reduce testing time.

This paper presents an oveview of techniques that have the potential to contribute to these objectives. Section 2 discusses the backgound and motivation for research activity in this area. Section 3 defines the concepts of DfT. Section 4 presents a survey of various DfT techniques, illustrating their capabilities and limitations. Pros and cons of different approaches are discussed in Section 5.

2: Background and Motivation

The motivations to employ DfT strategies in IC design are not obvious at the first glance. Add-on test circuitry does not improve the primary circuit functions. It does not make a circuit faster, it does not reduce the power consumption, and it does not make it more robust to variations of process or environmental parameters.

Even worse, the circuitry for testing adds additional problems. Circuit performance is degraded by for example switching elements in signal paths. The chip complexity

increases. The "beauty" and "elegance" of a particular circuit solution is often questionable after test circuitry has "ruined" the layout (this is a point to which especially analogue designers react very sensitively).

The absolute worst case for an analogue designer seems to be a DfT approach which involves a completely new design strategy. A DfT strategy which is not merely an add-on module to an existing (and working) circuit solution but is dominantly shaping the silicon solution (by for example determining the module boundaries) seems to bring limitations and restrictions to the freedom of the analogue designer (and the circuit implementation) which are often expressed to be "unbearable".

And on top of all, every DfT approach requires additional circuitry which increases the chip area, therefore increasing the die manufacturing costs and increasing the probability of faults in the chip (through increased die size).

So, why worrying about DfT at all?

The driving force to utilise DfT strategies for analogue and Mixed Signal ICs comes from market demands. One main reason for DfT is to reduce the (final) costs of ICs through reducing testing time. Testing a mixed-signal chip after production is responsible for between 30 and 80% of the total cost, depending on chip system complexity, volume, and applicational demands.

Furthermore, DfT increases the testability (per definition) and, therefore, increases the fault coverage which in turn increases the reliability of a circuit in the field by reducing early life failures. In the opinion of the authors:

"The current trend in the IC industry towards "single figure ppm levels" necessitates the integration of DfT strategies to support high fault coverage and low cost production test with minimal performance penalties to maintain the competitive edge."

A third reason to employ DfT for ICs are demands from safety critical, highly dependable, or highly reliable applications. Complex solutions for the health, the nuclear, or the transportation industries (including automotive, aerospace and public transportation applications) demand high testability and (on-line) functional verification to allow safe, dependable and reliable operation. Furthermore, legislative requirements and demands from insurers in many cases necessiate proof on "completeness" in testing after manufacture and even on-line verification capabilities for certain applications [17].

DfT emerges from a mere idea to make the test engineers life easier to a concept which is paramount to successful IC design, production, marketing, and sales.

3: The concepts of Design-for-Test (DfT)

What is the definition of Design for Test or Design for Testability? What techniques does the *DfT* acronym embrace?

Williams and Parker [18] describe DfT as follows:

"The collection of techniques that comprise Design for Testability are, in some cases, general guidelines; in other cases, they are hard and fast design rules. Together they can be regarded essentially as a menu of techniques, each with its associated cost of implementation and return on investment".

An alternative definition proposed by the authors is;

"To support the implementation of IC test capable of satisfying the demands on exhaustiveness and associated cost such as testing time, circuit overhead, and tester requirements for competitive, marketable products.

An important issue on improving testability is the accessibility of nodes. Submicron technologies allow us to integrate millions of transistors into a single chip. How can we ensure that every component is working? Techniques on how to inject signals into embedded modules/nodes (controllability) and on how to access the (test) response (observability) with adequate resolution are essential for this purpose. Other major concerns are the 'isolation' of circuit modules (to fully exploit digital testing techniques) and the possibility of testing analogue functions separately.

The 'continuous' and 'distributed' nature of signals is particular to analogue circuits. For this reason, analogue DfT differs from digital DfT (as analogue design differs form digital design).

4: Design-For-Test Approaches

Fig. 1 groups various techniques for DfT in six clusters and gives examples. Despite the differences in their approach they all have the same aim of improving the testability of IC designs.

4.1: Rules and Guidelines

Most DfT rules and guidelines to improve testability are 'good practice' or 'common sense' knowledge on circuit design gathered from previous experience [1]. A set of general principles has been developed [19], quite similar to the 'ad-hoc' testing techniques in digital design:

- Partition the circuit in macro blocks;
- Control macro inputs;
- Observe macro outputs;
- Disable feedback paths;
- Place digital storage elements at A/D and D/A interfaces;
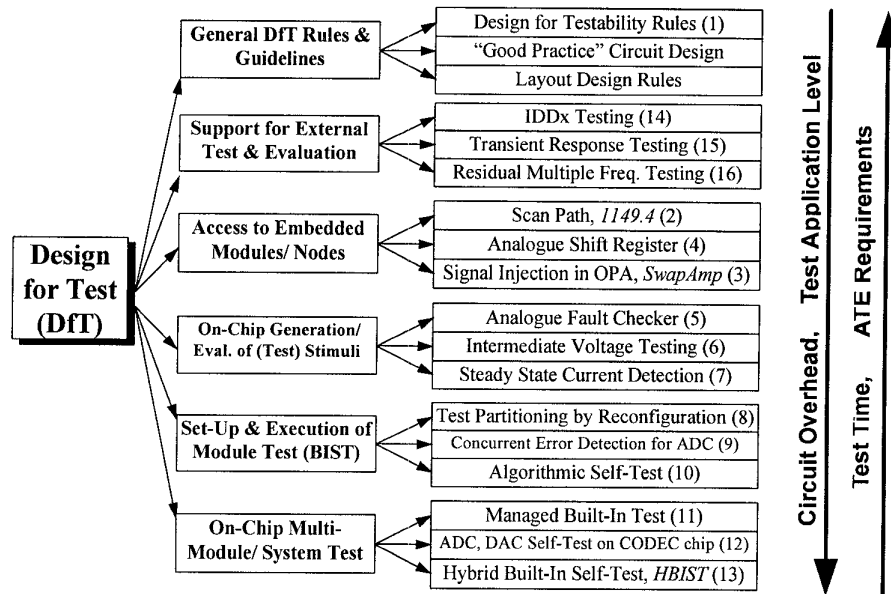- Use digital digital test access port to select test mode.

Figure 1: Various Design for Test (DfT) techniques and implementation examples

These guidelines can also be integrated in CAD tools and monitored via design rule checkers.

4.2: Support for External Test

Support for external test and evaluation is an important application of DfT.

Power supply current monitoring or I_{DDQ} testing [20] has become a standard test technique in industry for digital designs. It may well be feasible to use the technique on mixed signal devices where appropriate circuit partitioning strategies are applied to ensure that analogue sections are either isolated (eg. separate power supplies) or test modes are used (where for example analogue modules are set into a sleep mode) to ensure the analogue circuitry has negligable effect on current levels during digital I_{DDQ} test. Various forms of current testing have been investigated for analogue circuitry. Process variations in certain analogue components, particularly the bias chains can cause wide variations in fault-free current levels that can effectively mask many fault effects [14]. Possible solutions have been proposed including taking two supply current measurements for two "opposite polarity" input signals, and processing the results so that the bias current component is effectively cancelled. [21]. It may also be feasible for certain circuits to include additional current mirror structures to effectively mirror the bias current for an anaolgue block to an additional probe pad. This would be a form of DfT or partial replication and could be used to provide access to the bias current for the analogue blocks during probe test.

Other 'external' testing techniques in this category are Transient Response Analysis [15] and Residual Multiple Frequency Testing [16].

Transient Response Analysis requires the introduction of a special interface scan structure between analogue and digital subsystems. The analogue part is excited with impulses and
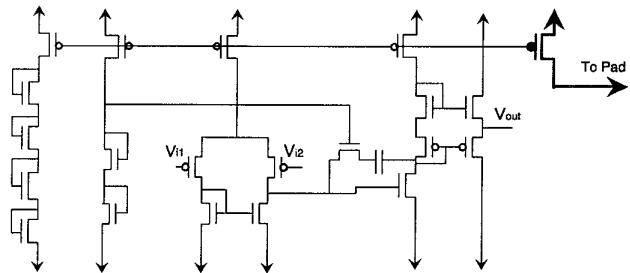

Fig. 2 - Additional mirror structure on Asymmetric OTA.

its output is digitised and processed to evaluate the frequency behaviour.

Residual Multiple Frequency Testing is suitable for linear analogue blocks with bandpass frequency response. Two sinusoidal signals are used, which lie just above and just below the operation bandwidth. By retrieving the amplitudes of test signals at the analogue output, faults can be detected. It is worth mentioning that this technique can be used also for concurrent testing, provided that test signals do not interfere with normal operation (ie. their amplitudes do not saturate

the circuit, no harmonic / subharmonic frequencies are generated, and analogue output is bandpass filtered to remove test signals).

4.3: Access to Embedded Blocks

Techniques for increasing controllability and observability with adequate resolution are catagorised under this section. Scan path [1] and the IEEE 1149.4 standard proposal [14] are examples for structured approaches to access embedded modules or nodes. IEEE 1149.4 is the analogue extension of IEEE 1149.1 Digital Boundary Scan architecture. The existing standard proposal is fully compatible with its digital counterpart, thus making possible to test mixed systems with a unified Test Access Port (TAP). The pin overhead is minimum (one analogue input and one analogue output besides the digital TAP). However, for certain applications where the total pin count is relatively low (especially consumer products) it may not be feasible to assign six or more pins to test.

One possibility to access embedded nodes without the need for analogue test pins is to use converters on-chip so that the tester interfaces the Circuit Under Test (CUT) in the digital domain. ADC and DAC in the test circuitry are then required to convert the digital serial I/O stream into analogue test signals [22]. One alternative to save the chip area for these converters at the expense of an additional analogue test pin are analogue shift registers [4].

Besides the requirements to establish a path to embedded nodes, there must be interfaces to inject test signals into the signal path circuitry and the 'swap amp' is one solution that causes only minimal degradation on the primary functions [3]. The 'swap amp' (Fig 3). is a configurable op-amp which can either operate in normal mode or act as a buffer for test signals. By selecting the appropriate 'swap amp' for test input, it is possible to inject test signals at almost any point in the analogue subsystem.

Further applications of the swap-amp have been proposed by huertas et al. [23]. Here all operational amplifiers are replaced by "swap-amps". All stages except the stage under test are put into test mode (op-amps in unity gain configuration). The input to the stage under test will then be equal to the primary input and the output of the stage under test will be propagated through subsequent stages to the primary output. This technique has been applied to a second order active RC filter and a second order SC filter.

4.4: On-Chip Test Evaluation

Off-chip test signal generation and evaluation imposes severe restrictions on the test signal itself. The maximum frequency, the signal amplitude, or the resolution of the test signal are limited by the clock rates of the digital serial chains, converters, or by chain elements in the analogue shift
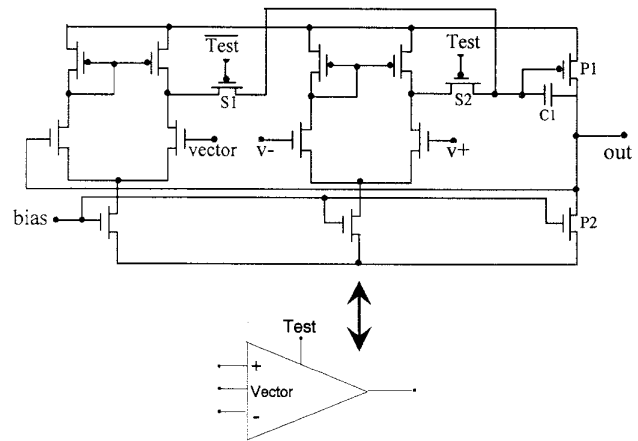

Fig. 3 - The swap-amp or re-configurable operational amplifier

registers. The quality of the test stimuli and response is limited by the links from the Automated Test Equipment (ATE) to the chip periphery and from the pins to the embedded modules/ nodes.

The alternative is to generate/evaluate (test) signals on-chip. Here, test information from the tester (or higher level systems) is decoded/coded and/or decompressed/compressed. This frees the external tester from dealing with 'difficult' analogue patterns at the expense of additional on-chip circuit overhead. Three examples are given for this DfT technique in Fig. 1.

The analogue fault checker [5] monitors inputs/outputs of fully differential circuits and uses relative tolerances for self-test evaluation. It has a negligible impact on area and circuit performance. Since it monitors the average value of differential signals, its application is limited to differential circuits; moreover, it can not detect 'symmetric' faults (e. g. differential bridging).

Intermediate voltage testing detects the forbidden zones between logical low and high level of digital outputs and sets flags to indicate a go/no-go signal [6].

Steady state current detection methods use built-in current monitors to evaluate the quiescent current between transitions in digital circuit modules in order to detect stuck-at and bridging faults [7].

Since fault sensitivities of voltage and current test are different, the two techniques can be used together to achieve an optimum fault coverage.

4.5: Built-In Self-Test

A further step to more on-chip integration can be achieved by utilising module level test that is completely self-contained

without any further off-chip support than the signal to trigger the Built-In Self-Test (BIST). Advantages here are that the test is customised and optimised to the CUT and that set-up and performance requirements for the external tester are drastically reduced. Testing time can be reduced through parallel execution of self-tested modules. The main disadvantages are the 'explosion' in circuit area associated to the self-test and the corresponding limitations on signal processing (i. e. you can not process a FFT with only five transistors).

Three examples are given here. The first one is a self-test plus evaluation by performing comparisons on reconfigured identical circuit modules (biquad filter elements) [8].

The second example for BIST on a module level is the utilisation of a time redundancy scheme to compare the conversion result of an ADC with a second 'sign inverted' one [9].

For the third example, an algorithmic self-test is used for a divide-by-two circuit. Here a reference current generator provides the input vector and DfT circuitry subtracts twice the output current from the original input current [10].

on-chip (self-) test	off-chip test
+ faster to execute	− higher testing time
+ on-line test possible	− only for manufacturing tests
− high chip-area overhead	
	− access to internal nodes difficult
− limited to simple measurements	+ complex measurements and evaluation possible
− higher initial costs for design	− increased testing time
+ only standard ATE required	− specialised, expensive ATE required
+ robust measurements possible due to close proximity	− parasitic capacitances − noise problems

Table 1: Trade-offs between on-chip self-test generation and evaluation and off-chip tests

4.6: On-Chip Multi-Module System Test

Submicron processes allow the integration of complete systems consisting of converters, filters, Digital Signal Processing (DSP) cores etc. on a single chip. The idea to utilise the on-chip processing power (in the form of microcontroller or DSP cores) to perform tests on other modules such as filters or converters allows 'Hierarchical Managed Built-In Test' [11]. where the interface message for

the request would be "Are you fault free?" and the chip-system response would be "Yes, I am fine!" (within certain resolution limitations)

Examples are presented by Ohletz with HBIST [13] and with an ADC, DAC self-test on a CODEC chip [12]. These system test approaches are in line with the concepts of modularity which are envisaged in smart sensors or microsystems [24].

5: Discussion

The more self-test functions that can be integrated onto a chip, the higher the associated circuit overhead. Integrated self-test is for certain applications the option to competitive solutions because of the advantages in test exhaustiveness, reduced testing time and effort, and the (possible) on-line self-test capability.

Techniques which enhance accessibility to embedded nodes may help to achieve the goals of controllability and observability with a lower overhead but leave the burden of analogue test generation and evaluation to the test equipment.

The more on cost for the design of self-test circuitry is traded off against the additional effort to set-up, run and maintain the ATE.

For each specific application, there is a compromise to make on which DfT technique to choose. The optimum solution might be in utilising the advantages of several DfT techniques.

The trade-offs between on-chip self-test generation and evaluation and off-chip tests which require circuitry to access embedded modules are listed in Table 1.

It is concluded that on-chip test approaches (and/or their partial implementations) are more applicable if not essential for complex mixed-signal systems, especially for safety critical applications. Off-chip tests still seem attractive for standard, high volume products where the high costs for specialised test equipment can be justified. The QTAG initiative [25] which sets out to define a standard for an off-chip IDDQ current monitor is one example which follows the off-chip testing route. It is important to note that future mixed-signal systems will utilise both on-chip self-test as well as features to simplify off-chip test.

6: Conclusion

This paper discusses the motivations for employing DfT structures for analogue and mixed-signal circuits. DfT is a must for reliable but cost effective mixed signal circuits and systems.

Six different DfT approaches have been identified and discussed with implementation examples. They range from mere testability guide lines to approaches to increase

accessibility of embedded modules and to techniques where complete tests are performed on-chip.

There will be no such 'The Test Technique' for mixed signal circuits and systems. Each application places special demands on the test requirements. The optimum testing strategy for a particular mixed-signal chip will be the synthesis of maybe several test approaches classified in this paper.

7: Acknowledgements

8: References

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