A Nested Digital Delta-Sigma Modulator Architecture for Fractional-N Frequency Synthesis

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Abstract—A nested digital delta-sigma modulator (DDSM) architecture for fractional-N frequency synthesis is investigated and compared with the conventional MASH 1-1-1 DDSM. In the nested architecture, the LSBs of the input word are processed by a first-order DDSM and added to the MSBs before being processed by a third-order DDSM. Using the error masking design methodology [1], rules for selecting the optimum wordlengths are presented. We show that the nested architecture requires 15% fewer flip-flops and 13% fewer full-adders than the conventional architecture, resulting in an overall hardware saving of 15%. Simulation results confirm the analytical predictions.

I. INTRODUCTION

Digital delta-sigma modulators (DDSMs) are key components in a wide range of modern communications products employing frequency synthesizers such as cellular telephones, wireless LANs and modems. In comparison with integer-N phase-locked loops (PLLs), fractional-N PLLs based on digital $\Delta\Sigma$ modulators can achieve very fine frequency resolution without the need for using low reference frequencies. The unfavorable trade-off between bandwidth and frequency resolution associated with integer-N PLLs is avoided at the expense of additional phase noise [2].

Figure 1 shows a block diagram of a typical $\Delta\Sigma$ fractional-N PLL consisting of a phase-frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a voltage controlled oscillator (VCO), a frequency divider, and a DDSM [3]. The input to the DDSM is an N-bit digital word X which sets the desired fractional division ratio $\frac{X}{2^N}$. The DDSM output is an integer-valued sequence $y[n]$, which is used to modulate the instantaneous division ratio of a frequency divider such that an average division ratio of $N + \frac{X}{2^N}$ is obtained over time. The quantization noise produced by the DDSM is high-pass shaped and subsequently removed by the PLL loop filter, thereby ensuring that the phase noise in the vicinity of the carrier is small.

Higher order DDSMs are typically employed in fractional-N PLLs in an effort to minimise the effect of the spurious tones (spurs) which usually are present in the DDSM output spectrum. Higher order DDSMs can be realized using interpolative or cascaded architectures. The design of single-loop high-order modulators can be problematic due to stability concerns [1]. Multi stAge noise SHaping (MASH) DDSMs, on the other
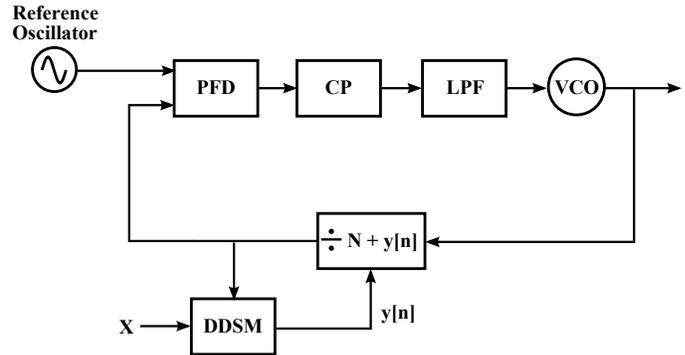
Fig. 1. Block diagram of a typical fractional-N PLL

hand, utilize a cascade of lower order modulators and are unconditionally stable.

Previous work in the area of D/A conversion has identified architectures in which the hardware complexity of the DAC can be reduced without sacrificing performance [4], [5]. This is achieved by using a DDSM to shape the LSBs of the input signal, thereby reducing the bit width of the DAC data path. In this work, we investigate this idea from the point of view of DDSMs to determine if similar hardware savings can be achieved. We address the MASH 1-1-1 DDSM which is a popular structure that offers full coverage of the fractional input range [6]. We investigate a novel architecture, the nested 1-3 DDSM, in which the input digital word is partitioned and applied to two different DDSMs. We compare the hardware complexity of the conventional MASH 1-1-1 DDSM and the nested 1-3 DDSM and show that the latter requires less area.

II. CONVENTIONAL MASH 1-1-1 DDSM ARCHITECTURE

Before we describe the nested architecture, we first review the conventional MASH 1-1-1 DDSM. This structure is based on the digital accumulator model shown in Fig. 2. The input to the accumulator is a digital word with N bits. The quantizer block $Q(\cdot)$ simply passes the MSB of $v[n]$ to the output $y[n]$ and the discarded LSBs are then fed back and summed with
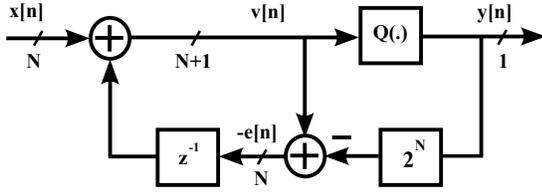
Fig. 2. Block diagram of a first-order error feedback modulator (EFM1)
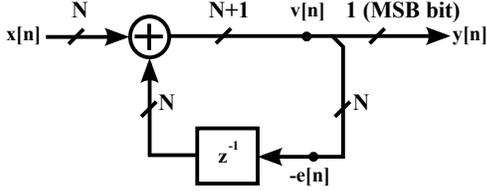
Fig. 3. Signal-flow graph of EFM1

the input. Mathematically, we can write

$$y[n] = \begin{cases} 0, & v[n] < 2^N, \\ 1, & v[n] \geq 2^N. \end{cases} \tag{1}$$

In the Z-domain, we can write the output, $Y(z)$, in terms of $X(z)$ and $E(z)$ as follows:

$$Y(z) = \frac{X(z)}{2^N} + \frac{(1 - z^{-1})E(z)}{2^N}. \tag{2}$$

This structure is referred to as a first-order error feedback modulator (EFM1). The signal flow graph of the EFM1 is shown in Fig. 3 [7]. Note that the implementation of an N-bit accumulator requires N flip-flops and N full-adders.

A MASH 1-1-1 DDSM is comprised of a cascade of three EFM1 blocks and a noise cancellation network, as shown in Fig. 4. In this structure, the negative of the quantization error from each stage ($-e_i[n]$) is fed to the next stage and the output of each stage ($y_i[n]$) is fed to the noise cancellation network, which eliminates the intermediate quantization noise terms. The output of the MASH 1-1-1 DDSM can be expressed in the Z-domain as:

$$Y(z) = \frac{X(z)}{2^N} + \frac{(1 - z^{-1})^3 E_3(z)}{2^N}, \tag{3}$$

where $X(z)$ and $E_3(z)$ are the Z-transforms of the input and the quantizer error introduced by the third stage. It can be shown [8] that a two's complement implementation of the noise cancellation network requires 4 flip-flops and 12 full-adders. The number of flip-flops and full-adders required to implement a conventional N-bit MASH 1-1-1 DDSM can therefore be written as

$$n_{FA,conv} = 3N + 12 \tag{4}$$
$$n_{FF,conv} = 3N + 4 \tag{5}$$
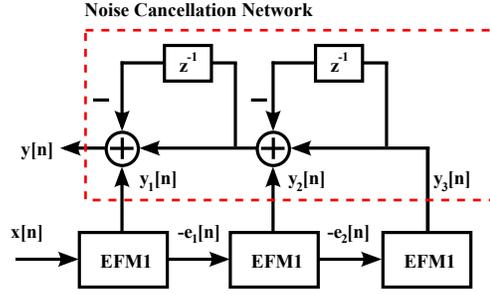
Fig. 4. Block diagram of a MASH 1-1-1 DDSM

III. NESTED ARCHITECTURE

A nested DDSM [4] divides the N bits of the input into multiple segments. Consider the architecture of Fig. 5, which we will refer to as a nested 1-3 DDSM. In this scheme, the input word is divided into 2 parts; the N_{MSB} most significant bits X_{MSB}, and the N_{LSB} least significant bits X_{LSB}. The N-bit input can be written as

$$X = X_{MSB} \cdot 2^{N_{LSB}} + X_{LSB}, \tag{6}$$

where

$$N = N_{MSB} + N_{LSB} \tag{7}$$

X_{LSB} is applied to a first-order DDSM (DDSM1) which produces a single bit output i.e. either 0 or 1. At the output of the DDSM1, we can write

$$Y_1(z) = \frac{X_{LSB}(z)}{2^{N_{LSB}}} + \frac{(1 - z^{-1})\epsilon_Q(z)}{2^{N_{LSB}}}, \tag{8}$$

where $\epsilon_Q(z)$ is the Z-transform of the quantization error of the DDSM1. This bit is then added to X_{MSB} giving

$$X_3(z) = X_{MSB}(z) + \frac{X_{LSB}(z)}{2^{N_{LSB}}} + \frac{(1 - z^{-1})\epsilon_Q(z)}{2^{N_{LSB}}}.$$

Note that this addition does not require the explicit implementation of an extra adder. It can be implemented by applying the output of the DDSM1 to the carry input of the first accumulator of the DDSM3. Using this method, it is possible to add the two signals without increasing the hardware cost. At the output of the DDSM3, we have

$$\begin{aligned} Y_3(z) &= \frac{X_{MSB}(z)}{2^{N_{MSB}}} + \frac{X_{LSB}(z)}{2^{N_{LSB}} \cdot 2^{N_{MSB}}} \\ &+ \frac{(1 - z^{-1})\epsilon_Q(z)}{2^{N_{LSB}} \cdot 2^{N_{MSB}}} + \frac{(1 - z^{-1})^3 E_3(z)}{2^{N_{MSB}}}, \end{aligned} \tag{9}$$

which, after simplification, yields

$$Y_3(z) = \frac{X(z)}{2^N} + \frac{(1 - z^{-1})\epsilon_Q(z)}{2^{N_{LSB}} \cdot 2^{N_{MSB}}} + \frac{(1 - z^{-1})^3 E_3(z)}{2^{N_{MSB}}}. \tag{10}$$

Note that in comparison with Eq. (3), the output of the nested 1-3 DDSM contains an additional shaped noise term which is scaled by a factor $1/2^{N_{MSB}}$. The number of flip-flops and full-adders required to implement the nested 1-3 DDSM is given by

$$n_{FA,nested} = N_{LSB} + 3N_{MSB} + 12 \tag{11}$$
$$n_{FF,nested} = N_{LSB} + 3N_{MSB} + 4 \tag{12}$$
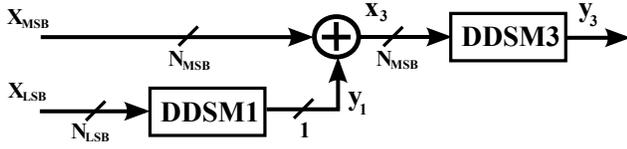
Fig. 5. Block diagram of the nested 1-3 DDSM

IV. DESIGN METHODOLOGY

The DDSM quantization noise power is spread over a number of tones that is determined by the cycle length, resulting in a tone spacing of $\Delta f = f_s/L_s$, where f_s is the sampling frequency and L_s is the cycle length. The locations of these tones are given by

$$f[k] = k\Delta f, \qquad k = 1, 2, \cdots, \frac{L_s}{2} \qquad (13)$$

where k is the index of the tone [1]. Assuming a cycle of length L_s and additive uniformly distributed white quantization noise, the idealized power spectrum of the shaped noise $NTF(z) \cdot \epsilon_Q$ is given by

$$S(f[k]) = \frac{1}{12L_s}|NTF(z)|^2_{z=e^{j2\pi k/L_s}}. \qquad (14)$$

Throughout this paper, we will use the power spectrum S_i that is obtained by assuming that the quantization noise E_i is white, to estimate the power spectrum of the actual shaped quantization noise component N_i. The output of the nested 1-3 DDSM can be written as

$$Y_3(z) = \frac{X(z)}{2^N} + \frac{N_1(z)}{2^{N_{MSB}}} + N_3(z), \qquad (15)$$

where $N_1(z) = (1-z^{-1})\epsilon_Q/2^{N_{LSB}}$ is the shaped contribution of the quantizer in the first order DDSM and $N_3(z) = (1-z^{-1})^3 E_3(z)/2^{N_{MSB}}$ is the shaped contribution from the quantizer in the third order DSDM.

Assuming that all quantization noise terms can be modeled as independent additive white sources and considering the weighting factor, we estimate the power spectrum of $N_1(z)$ as

$$S_1(f[k]) = \frac{1}{12L_1}\left(\frac{1}{2^{N_{MSB}}}\right)^2 \left|(1-z^{-1})\right|^2_{z=e^{j2\pi k/L_1}}, \quad (16)$$

where L_1 is the cycle length of the error signal from the first order DDSM. By setting the least significant bit (LSB) of the input to 1, L_1 is equal to $2^{N_{LSB}}$ [10]. In the same manner, by assuming a white error source $E_3(z)$, we estimate the power spectrum of $N_3(z)$ as

$$S_3(f[k]) = \frac{1}{12L_s}\left|(1-z^{-1})^3\right|^2_{z=e^{j2\pi k/L_s}}, \qquad (17)$$

where L_s is the cycle length which is $2^{N_{MSB}+N_{LSB}}$. The idea of the wordlength selection strategy is to mask the contribution of the intermediate quantizer by hiding the noise component N_1 below the N_3 component. The spectral envelope S_1 due to the first order DDSM should lie below the S_3 envelope.

Since both are discrete spectra, the constraints apply at a finite number of points. In particular, we require that:

$$S_1 \le S_3 \ @ \ f = f_s \cdot k/L_1, k = 1, 2, ..., L_1/2 \qquad (18)$$

Recall that, for a DDSM with an output cycle length of L_s, the lowest frequency tone is at f_s/L_s. Therefore, since the cycle length for N_1 is $2^{N_{LSB}}$, the lowest frequency tone in the power spectrum of N_1 is at $f_s/2^{N_{LSB}}$.

Additionally, at the output of the nested 1-3 DDSM, since S_1 is first-order shaped, while S_3 is third-order shaped, if the level of the lowest frequency tone in N_1 is below that of N_3, the overall power of N_1 should always be below the S_3 envelope. Based on this idea, the constraint can be rewritten as:

$$S_1 \le S_3 \ @ \ f = f_s/2^{N_{LSB}}. \qquad (19)$$

Since

$$\begin{aligned}\left|1-z^{-1}\right|^2 &= \left|1-e^{-j2\pi f/f_s}\right|^2 \\ &= \left|2\sin(\pi f/f_s)\right|^2\end{aligned} \qquad (20)$$

and

$$\sin(\pi f/f_s) \approx \pi f/f_s \quad \text{for} \quad f << f_s, \qquad (21)$$

we can approximate S_1 and S_3 at low frequencies by

$$S_1 \approx \frac{1}{12L_1} \cdot \left(\frac{1}{2^{N_{MSB}}}\right)^2 \cdot 2^2(\pi f/f_s)^2, \qquad (22)$$

$$S_3 \approx \frac{1}{12L_3} \cdot 2^6(\pi f/f_s)^6. \qquad (23)$$

Substituting Eqs. (22)−(23) into (19), we obtain

$$\begin{aligned} &\frac{1}{2^{2N_{MSB}}} \cdot \frac{1}{12 \cdot 2^{N_{LSB}}} \cdot 2^2 \cdot \frac{\pi^2}{(2^{N_{LSB}})^2} \\ &\le \frac{1}{12 \cdot 2^{N_{LSB}+N_{MSB}}} \frac{2^6\pi^6}{(2^{N_{LSB}})^6}\end{aligned} \qquad (24)$$

which reduces to

$$4N_{LSB} - N_{MSB} \le 10.6. \qquad (25)$$

If we define $N = N_{MSB} + N_{LSB}$ and $M = N_{MSB}$, then substituting into and simplifying Eq. (25) yields

$$M \ge 0.8N - 2.12. \qquad (26)$$

If the wordlength N of the input is known, M can be calculated from (26). Therefore, the optimized values of N_{MSB} and N_{LSB} can be calculated using

$$\begin{aligned} N_{MSB} &= M, \qquad (27) \\ N_{LSB} &= N - M. \qquad (28)\end{aligned}$$

Based on Eqs. (26)–(28), in order to design a nested 1-3 DDSM with the same cycle length and similar power spectrum as a conventional N_0-bit MASH 1-1-1 DDSM, the design procedure is as follows:

1) Choose $N = N_0 + 1$ to ensure that the cycle lengths of the conventional and nested 1-3 DDSM are equal;
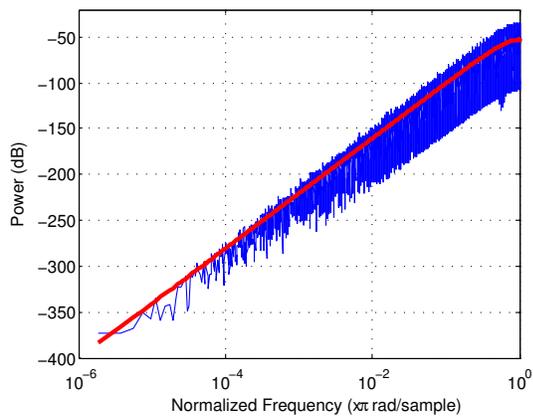
Fig. 6. Simulated discrete output power spectrum for a conventional 19-bit MASH 1-1-1 DDSM; the input is 157287. The smooth curve is S_3 (17).

Fig. 7. Simulated discrete ouput power spectrum for a 14-6 bit nested 1-3 MASH DDSM; the input is 314573. The smooth curve is S_3 (17).

TABLE I
HARDWARE CONSUMPTION OF THE CONVENTIONAL 19-BIT MASH 1-1-1 DDSM AND THE NESTED 1-3 DDSM WITH N_{MSB}=14 AND N_{LSB}=6

MASH DDSM	Hardware Consumption		
	FFs	LUTs	TEGs
(a) Conventional 19-bit	61	69	1229
(b) 14-6 bit 1-3 nested	52	60	1049
((b)/(a))%	85%	87%	85%

2) Choose $M = \lceil 0.8N - 2.12 \rceil$, where $\lceil x \rceil$ denotes the smallest integer greater than x. This ensures that the power of the first tone of N_1 is less than S_3 at the frequency $f_s/2^{N_{LSB}}$;

3) Choose N_{MSB} and N_{LSB} using (27) and (28).

V. DESIGN EXAMPLE

We present a design example for a 19-bit MASH 1-1-1 DDSM in order to verify the design methodology. The required wordlengths given by Eqs. (26)–(28) are $N_{MSB} = 14$ and $N_{LSB} = 6$. The inputs are chosen as the odd numbers that set the normalized input as close as possible to the value 0.3; $X = 157287$ in the case of the conventional DDSM and $X = 314573$ in the case of the nested 1-3 DDSM. The output discrete power spectra of the conventional and nested 1-3 DDSM are shown in Figs. 6 and 7, respectively.

The hardware requirements for the conventional 19-bit MASH 1-1-1 DDSM and the nested 1-3 DDSM are summarized in Table I. The hardware consumption is reported as the number of flip-flops (FFs) and number of 4-input look-up-tables (LUTs). The total-equivalent-gate (TEG) count is given as well. These results are based on the map report from the Xilinx ISE program [11]. In terms of overall complexity, the 14-6 bit 1-3 nested DDSM requires 15% less hardware than the conventional 19-bit MASH 1-1-1 DDSM and has marginally better spectral performance.

VI. CONCLUSION

In this work, we have presented a novel architecture for reducing the hardware complexity of MASH DDSMs. Using a design methodology based on error masking [1], we have shown how to determine the optimum wordlengths for each stage of the nested 1-3 DDSM, which allows a reduction in the hardware complexity by 15%, without degrading the spectral performance.

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