A. Fornasari, P. Malcovati, F. Maloberti: "**Improved Modeling of Sigma-Delta Modulator Non-Idealities in SIMULINK**"; Proc. of the IEEE International Symposium on Circuits and Systems, ISCAS 2005, Kobe, 23-26 May, Vol. 6, pp. 5982-5985.

Improved Modeling of Sigma-Delta Modulator Non-Idealities in SIMULINK

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***Abstract*—The goal of this paper is to present an extension of the behavioral models, implemented in the Matlab/Simulink™ environment, previously presented in [1, 2] and available in [3]. This toolbox allows us to simulate at behavioral level most of the switched-capacitor (SC) sigma-delta (ΣΔ) modulator non-idealities, such as sampling jitter, kT/C noise and operational amplifier limitations (finite bandwidth, finite DC gain, slew rate and saturation). Although very effective in simulating wide-band, medium-resolution ΣΔ converters the lack of a model for flicker noise and multi-bit quantizers makes this toolbox less attractive for simulating narrow band high resolution converters. The proposed extension not only fixes this limitation, but introduces a predictive model of the effect of capacitor mismatch in the internal multi-bit D/A converter.**

I. INTRODUCTION

Due to the inherent non-linearity of the sigma-delta (ΣΔ) modulator loop, the optimization of the basic building blocks has to be carried out with behavioral time-domain simulations [1]. The Matlab/Simulink® toolbox (SD Toolbox) presented in [1, 2] is a good trade-off between accuracy and speed of the simulations. In this paper two additional blocks are presented. The first allows us to include in the Matlab environment data about the noise power spectral density (PSD) of the operational amplifiers obtained by a circuit simulator (e.g. Spectre or Eldo), including flicker noise. The second one allows us to estimate the impact of the mismatches among capacitors in the feedback DAC of a multi-bit ΣΔ modulator on the signal-to-noise and distortion ratio (SNDR). In order to validate the proposed models, we simulated both at behavioral and transistor level the second-order switched-capacitor (SC) ΣΔ modulator architecture shown in Fig. 1 [4], which features a 12 levels internal DAC (11 comparators in the ADC).

II. NOISE MODEL

In the original toolbox (SD Toolbox) all the possible noise sources (mainly the contributions of the operational amplifiers and of the voltage references) were supposed to be white. The parameter V_n of the noise model (i.e. the noise rms voltage) had to be evaluated using a transistor-level noise simulation in the proper clock phase and including all the load capacitors. The output referred noise PSD obtained from the simulation had then to be integrated over the whole frequency spectrum, thus obtaining the total noise power V_n^2. The square root of this value, V_n, was finally used in the model to scale the output of a Gaussian distributed random signal. This model allows very fast simulations and can be used without any worry, if one of the two following considerations is satisfied:

- the flicker noise (1/f) can be neglected in the specific field of application (wide band converters);
- the noise spectrum is folded, due to sampling operation, a number of time sufficient to be considered white.

If these two conditions are not satisfied a more accurate model has to be used.

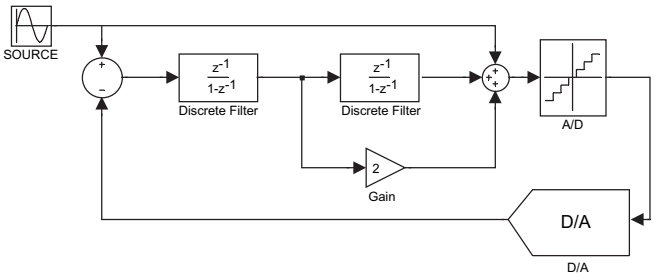

Figure 1. ΣΔ modulator topology porposed in [4] and used to test behavioral blocks.

III. COLORED NOISE MODEL

The noise PSD (expressed in V^2/Hz), provided by most transistor-level simulator, can be considered as the spectrum of the sum of N sine-waves with arbitrary phase (Fourier theorem), each having a power equal to the area of a slide of the PSD as large as F_{MAX} divided by N (i.e. as large as a bin)

$$V_{Noise} = \sum_{i=1}^{N} a_i \sin\left(2\pi \frac{F_{MAX}}{N} it + \varphi_i\right), \qquad (1)$$

This simple consideration is the basis for the proposed noise model, whose flow chart is shown in Fig. 2. Basically, we pass in the Matlab environment a detailed description of the noise PSD, elaborate it (basically folding it around the sampling frequency F_s) and calculate the value of V_{Noise} at the end of each clock period (T_s). The first possibility to pass the PSD in the Matlab environment is to sample the waveform (Fig. 3) provided by the transistor-level simulator (e.g. using the Ocean commands in the Cadence environment) and to reconstruct the function in Matlab. A simpler possibility is to

take advantage of the knowledge about the shape of the noise PSD. Considering that the noise power is additive, the PSD can be considered as the sum of a term due to flicker noise and one due to thermal noise, low-pass filtered by the circuit transfer function:

$$S_N = \left(c + \frac{k_1}{f} \right) \frac{1}{1 + f^2 / f_P^2} . \quad (2)$$

In this way, by providing the coordinates of only two points, the corner frequency (f_C, y_C) and the pole frequency (f_P, y_P), it is possible to estimate the parameters k_1 and c, according to

$$c = -\frac{-f_C^3 y_C - f_C f_P^2 y_C + 2 f_P^3 y_P}{(f_C - f_P) f_P^2}$$
$$k_1 = -\frac{f_C \left(f_C^2 y_C + f_P^2 y_C + 2 f_P^2 y_P \right)}{(f_C - f_P) f_P} \quad (3)$$

as shown in Fig. 3.

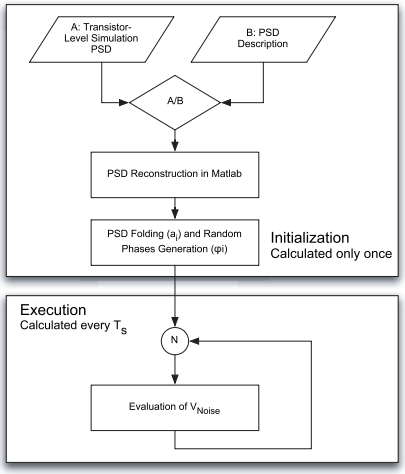

Figure 2. Flow chart of the proposed colored noise model.

Once obtained the analytic function of the noise PSD, it is possible to define its Fourier series. In order to reduce the complexity of the model, we calculate the impact of the sampling operation on the noise spectrum in the initialization phase, defining an equivalent envelope limited in the frequency range [0; F_s/2]. In this way it is possible to use a smaller number of sine-waves or, alternatively, to have a better frequency resolution with the same number of sine-waves (Fig. 4). All the code is written using vectorizing algorithms, i.e. carefully avoiding the use of "for" and "while" loops and replacing them with the equivalent vector or matrix operation. This allows to speed-up simulations [6].

Since with this model we can include the data coming form the circuit simulator, it is also possible to evaluate the impact of techniques as auto-zero or correlated double sampling (CDS) on the performance of the whole converter [5]. This can simply be accomplished by connecting at the output of the noise model block the proper z-domain transfer function.

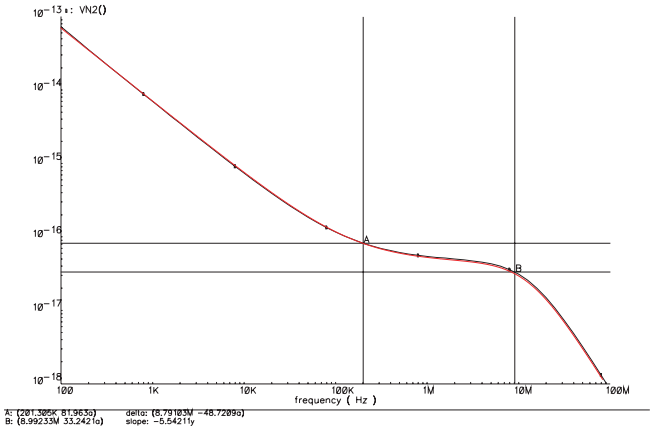

Figure 3. Noise output PSD of an operational amplifier obtained from a circuit simulator (black) and reconstructed by Matlab (red). The PSD integral on 1 GHz bandwidth is 1.089 nV^2, which means V_n=33 µV.

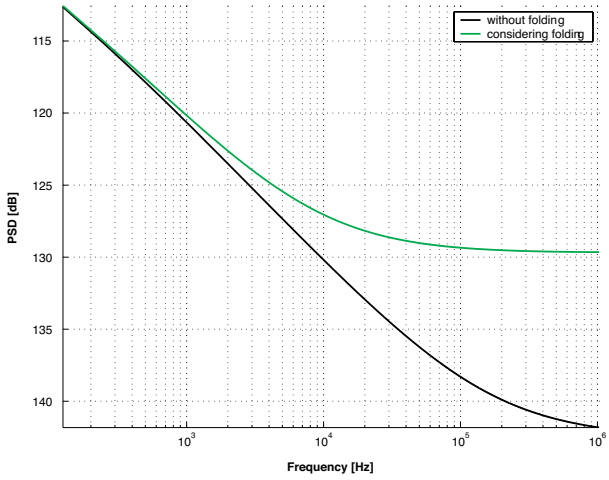

Figure 4. Noise output PSD in the band [0 F_S] before and after having considered the folding due to the sampling operation.

IV. Simulation Results

To validate the proposed model, we performed several simulations with Simulink using the model shown in Fig. 7 of the 2nd order modulator of Fig. 1. A sampling capacitor C_S of 12 pF was chosen. The circuit was simulated for two different values of the sampling frequency F_s (2.5 MHz and 1.25 MHz, assuming a jitter of 1‰ of the clock period) with different values of the oversampling ratio (OSR) to highlight the impact of 1/f noise in different operating conditions (Table 1 and Fig. 6). The different versions of the toolbox were compared initializing random generators with the same seeds to better evaluate the algorithms. As operational amplifier we used a simple differential pair with active load and a bias current of 40 µA, having a dc gain of 40 dB and a gain-bandwidth (GBW) product of 6 MHz. Its output noise PSD

has already been reported in Fig. 2. A transistor level noise simulation (in time domain) of the ΣΔ modulator with F_s=1.25 MHz and OSR=256 was made to verify the improvement in simulation accuracy of the proposed colored noise block.

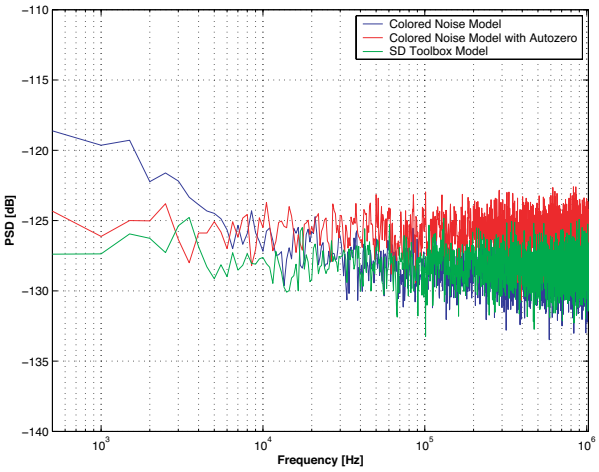

Figure 5. Noise output PSD modeled by the original (black) and the proposed block with (red) and without (green) autozero. The PSD was obtainded averaging ten FFTs on a window of 2^{15} points.

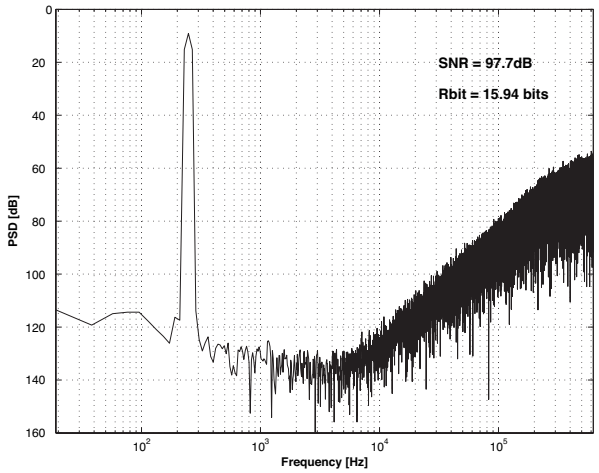

Figure 6. PSD of the 2nd order ΣΔ modulator with F_s=1.25 MHz and OSR=256. It is clearly visible the colored noise floor.

V. MULTI-BIT QUANTIZER MODEL

It is well known [5] that a mismatch among capacitors in the internal DAC of a multi-bit ΣΔ modulator causes an increase in the noise floor and in the harmonic distortion. Performance degradation is proportional to capacitor standard deviation (σ), given by:

$$\sigma\left(\frac{\Delta C}{C}\right)=\frac{k}{\sqrt{W\cdot L}}\left[\%/\mu m\right] \qquad (4)$$

TABLE I. SIMULATED PERFORMANCES

F_s=2.5 MHz		
OSR=512 Bandwidth=2.4 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	142.6	23.4
SD Toolbox	109.6	17.9
SD Toolbox update	99.4	16.2
SD Toolbox update w/ autozero	110.5	18.1
OSR=256 Bandwidth=4.9 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	129.1	21.2
SD Toolbox	108.3	17.7
SD Toolbox update	94.4	15.4
SD Toolbox update w/ autozero	105.4	17.2
OSR=64 Bandwidth=19.5 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	97.4	15.9
SD Toolbox	94.4	15.4
SD Toolbox update	94.4	15.4
SD Toolbox update w/ autozero	95.2	15.5
F_s=1.25 MHz		
OSR=512 Bandwidth=1.2 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	138.9	22.7
SD Toolbox	111.3	18.2
SD Toolbox update	97.7	15.9
SD Toolbox update w/ autozero	108.0	17.6
OSR=256 Bandwidth=2.4 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	129.1	21.2
SD Toolbox	106.4	17.4
SD Toolbox update	97.8	15.9
SD Toolbox update w/ autozero	105.6	17.3
Transistor-level noise simulation	96.2	15.7
OSR=64 Bandwidth=9.7 kHz		
Model	***SNR [dB]***	***Bit***
Ideal	98.6	16.1
SD Toolbox	95.9	15.6
SD Toolbox update	93.5	15.2
SD Toolbox update w/ autozero	95.3	15.5

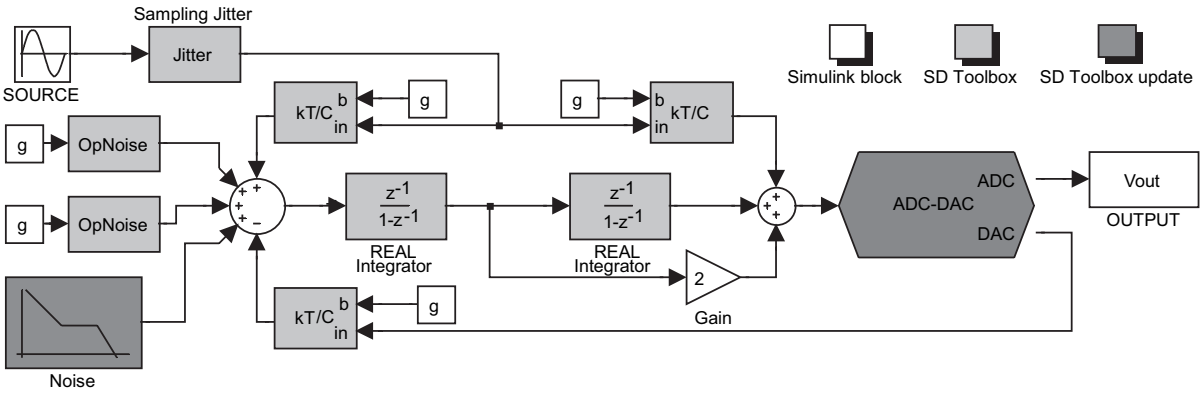

Figure 7. Simulink model of the ΣΔ modulator simulated with blocks introduced in the previous version of SD Toolbox and those proposed in this paper

Therefore, σ is inversely proportional to the square root of the capacitor size (the constant k depends on the technology and is usually provided by the silicon foundry). Considering that the sampling capacitor value impacts the constraints of almost all basic building blocks (e.g. operational amplifiers and voltage references) it has to be determined at the very beginning of the design phase. This makes approaches based on circuit simulator (e.g. Montecarlo simulation) ineffective (not only time consuming).

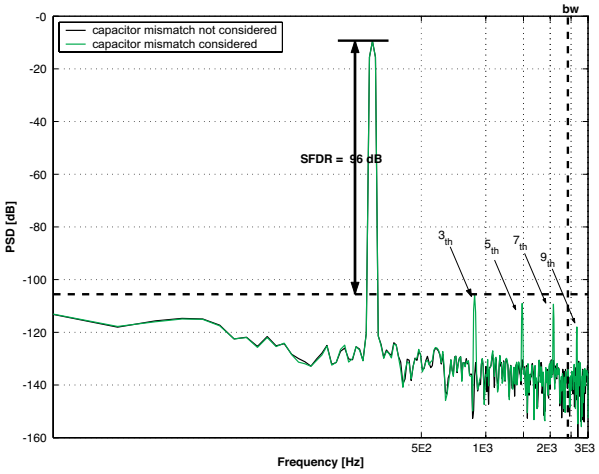

Figure 8. ΣΔ modulator output spectrum with and without capacitor mismatch. The FFT is performed on a window of 2^{17} points.

Therefore, we developed a block which models the ADC and DAC of a ΣΔ modulator, including the mismatch effects. This block can be used to evaluate if, given a sampling capacitor size, the performance degradation due to mismatch can be considered negligible with respect to thermal noise, or if some correction technique, e.g. dynamic element matching (DEM), has to be applied (Fig. 8). The internal DAC was supposed to have an odd symmetry (as it happens in reality in all fully differential circuits and in all single ended circuits carefully designed), which means that the same elements are used to construct both positive and negative values. Under this assumption no even distortion can be introduced by DAC. This shrewdness is fundamental to avoid overrating mismatch effect on the output spectrum.

CONCLUSIONS

In this paper we presented an extension of the SD Toolbox, which includes a more general noise model with also flicker noise and a multibit quantizer model considering capacitor mismatches. Transistor level simulation have demonstrated that, under specific conditions, the proposed noise model achieves results by far more accurate than the original one. Moreover, the multibit quantizer model allows us to accurately estimate the sampling capacitance value required for achieving a given harmonic distortion at the very early stage of the design.

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