

A 1.8 GHz CMOS Low-Noise Amplifier

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ABSTRACT

A 1.8 GHz low-noise amplifier has been designed and fabricated in a standard 0.35 μm CMOS process. Measurement results indicate that the amplifier has a forward gain (S_{21}) of 10.5 dB and a noise figure of 3.94 dB, while consuming 40 mW from a 2.5 V supply.

1. INTRODUCTION

The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages. Aside from providing this gain, while adding as little noise as possible, an LNA should accommodate large signals without distortion and frequently present a specific impedance, usually 50 Ω , to the input source. This 50 Ω impedance matching is particularly important if a passive filter precedes the amplifier, since the transfer characteristics of many filters are quite sensitive to the quality of the termination [1]. Since the LNA is the first gain stage in a receiver's path its noise figure adds to that of the system, hence a low noise figure is desired. This low noise requirement governs the choice of the topologies and parameter values employed in the design [2].

LNA design is full of trade-offs between optimum gain, lowest noise figure, input and output port matching, linearity and power consumption. At first sight the LNA might seem simple to design due the relatively few components used in its implementation but these trade-offs complicate the design. Also standard CMOS process inductors present a

low Q limiting the maximum achievable gain.

A 1.8 GHz low-noise amplifier designed using a standard double-poly triple metal 0.35 μm CMOS process is presented. The circuit uses the inductive degeneration technique to present a 50 Ω impedance at its input port. The circuit also uses a two-stage cascaded architecture to provide sufficient gain while presenting a good isolation between the input and output ports. This isolation is very important since it blocks the signal from returning to the antenna causing interference with the required signal. Measured results have shown that the circuit has a maximum gain of 10.5 dB at 1.8 GHz, a noise figure of 3.94 dB, and an input referred IP3 of -2.4 dBm while consuming 40 mW. The circuit description is presented in section 2. Measurement results follow in section 3, while a conclusion is given in section 4.

2. CIRCUIT DESIGN

2.1. Circuit Analysis

The schematic diagram of the designed LNA is shown in Fig. 1. In the analysis of this amplifier, the conditions that guarantee optimized noise performance for a fixed power consumption are taken. Since the architecture permits the selection of the quality factor, Q_L , and the source inductance L_S , independently, a solution exists for which the optimum noise performance coincides with the required 50 Ω input match.

The optimum width of the input transistor under these conditions can be found using [1]:

$$W_{opt} = \frac{2}{3\omega L C_{ox} R_s Q_s} \quad (1)$$

where ω is the frequency of oscillation, C_{ox} is the oxide capacitance, L is the effective length of the transistor and Q_s is the optimum quality factor. The optimum conditions are not extremely sensitive to the width since a variation of 20 % one way or the other will only degrade the noise figure by one or two tenths of a decibel [1].

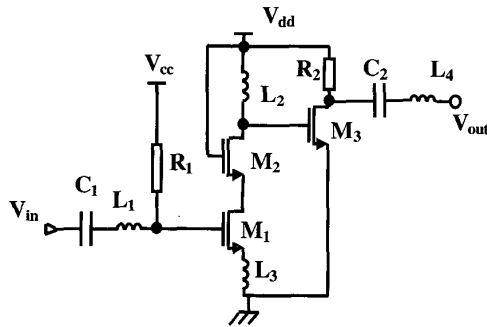


Fig. 1 – Schematic Diagram of the LNA

After calculating the optimum width of the device, the next stage is to design the input matching network. A simple analysis of the circuit depicted in Fig. 1 shows that the input impedance of the circuit is given by [3]:

$$Z_{in} = s(L_1 + L_3) + \frac{1}{C_{gs1}} + \frac{g_{m1}}{C_{gs1}} L_3 \quad (2)$$

The matching condition occurs when [4]:

$$\omega^2 C_{gs}(L_1 + L_3) \approx 1 \quad (3)$$

Thus at resonance (2) becomes:

$$Z_{in} \approx \frac{g_{m1}}{C_{gs1}} L_3 \quad (4)$$

where Z_{in} is equal to 50Ω , g_{m1} is the transconductance of transistor M_1 and C_{gs1} is the gate-to-source capacitance of transistor M_1 .

From the circuit diagram, shown in Fig. 1, it can be noticed that the center frequency of the narrow band low-noise amplifier is obtained by resonating the inductor L_2 with

the total capacitance at the drain of transistor M_2 and the C_{gs} of transistor M_3 . Capacitors C_1 and C_2 are coupling capacitors for dc isolation of the input and output ports. The output impedance is matched to 50Ω by using a common-source stage M_3 .

2.2. Circuit Realization

The width of the input transistor was calculated using (1) and taking Q_s to be equal to 6. This resulted in transistor M_1 having a width of $300 \mu\text{m}$. The biasing network was composed of a 1 V supply V_{cc} and a 70Ω resistor. Once this bias condition has been established the value of g_{m1} and C_{gs1} could be found. Applying these values in (4) and replacing Z_{in} by 50Ω results in 470 pH inductance value for L_3 . L_1 was then found to be equal to 6.5 nH using (3). Tuning of the input was done by varying C_1 .

The output was then tuned to a maximum gain at 1.8 GHz by varying the widths and lengths of transistors M_2 and M_3 , thus varying the capacitance seen by the 7 nH inductor L_2 . The width/length ratio of M_2 and M_3 were $400/1$ and $170/0.4$ respectively.

The amplifier was implemented and fabricated using a standard CMOS process. The inductors were designed using spiral metal 3 inductors. The metal 3 layer was used to reduce losses to substrate. These inductors were implemented using the following equation [1]:

$$L \approx \frac{45\mu_0 n^2 a^2}{22r - 14a} \quad (5)$$

where μ_0 is the permeability of free space, a is the square spiral's mean radius defined as the distance from the center of the inductor to the middle of the windings, n is the number of turns, and r is the radius of the spiral.

The inductance introduced by the bondwires was taken into account during the design of these inductors. This value of inductance is approximately 1 nH/mm of bondwire [1]. Also because of its small value inductor L_3 was implemented entirely in bondwire, and this was done by connecting several bondwires in parallel.

Interdigitated transistors were used in the

implementation in order to reduce their input resistance thus improving their noise performance. This also helps in reducing the total area occupied by the circuit. The layout of the low-noise amplifier occupies a total die area of $1025 \times 1345 \mu\text{m}^2$ and the chip micrograph is shown in Fig. 2.

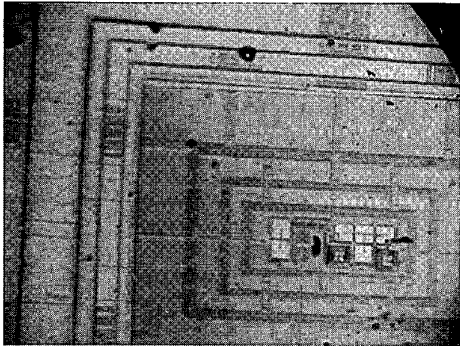


Fig. 2 – Chip Micrograph

3. MEASUREMENT RESULTS

The circuit was directly bonded on the PCB in order to reduce the losses introduced by the package. The tracks on the PCB were designed to present a 50Ω both to the source and to the load.

The S-parameters were measured using an HP 8719ES network analyzer and are shown in Fig. 3 and Fig. 4. Fig. 3 shows that the S_{11} and S_{12} parameters are at -8.4 dB and -41.7 dB , respectively. The measurements of S_{21} and S_{22} are given in Fig. 4 and the results are 10.5 dB and -6.6 dB , respectively.

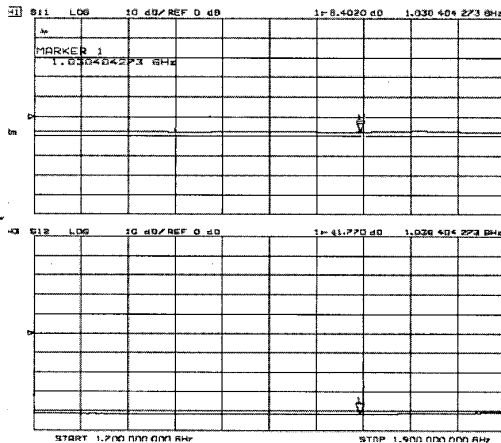


Fig. 3 – Measured S_{11} and S_{12}

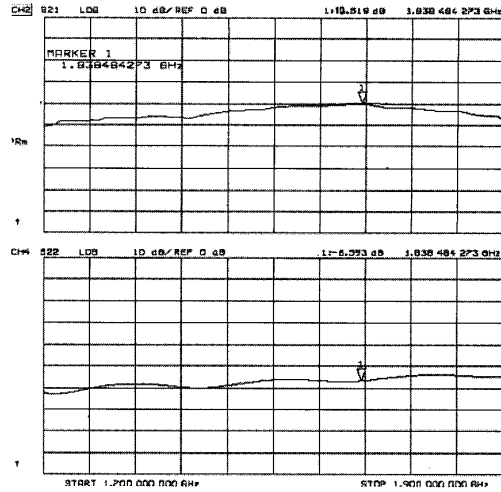


Fig. 4 – Measured S_{21} and S_{22}

The input was connected to a signal generator and the signal power was varied while keeping the operating frequency constant at 1.8 GHz . The fundamental output power together with the third harmonic output power were noted for each value of the input signal power using a spectrum analyzer. These results were plotted on a graph and the result is shown in Fig. 5. This shows that the input referred IP3 of the circuit is -2.4 dBm .

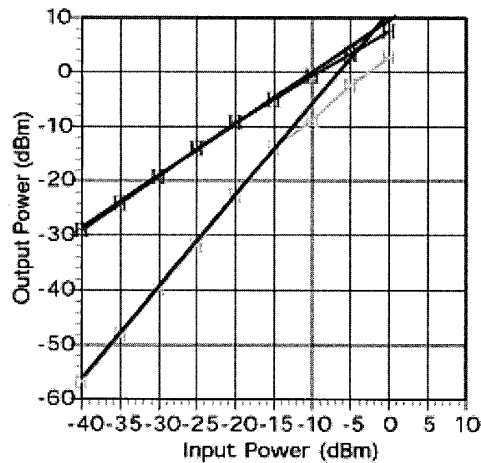


Fig. 5 – Measured IIP3

The measurement of the noise figure against frequency, illustrated in Fig. 6, shows that the LNA has a noise figure of 4 dB at 1.8 GHz . The measured power dissipation of the circuit is 40 mW when operated from a 2.5 V supply and a bias voltage of 1 V .

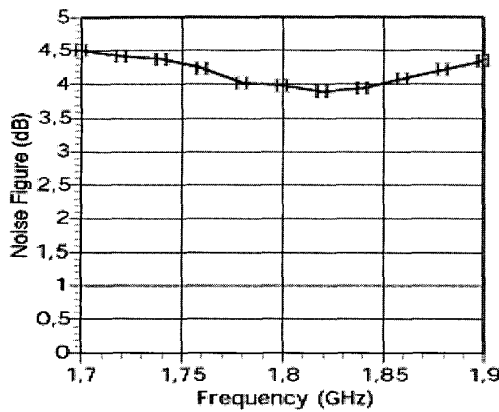


Fig. 6 – Measured Noise Figure

Table 1 shows a list of previously published results together with this implementation. These results indicate that the results obtained in this work are comparable to these implementations.

Table 1 - Comparison of LNAs

Author	Frequency	Noise Figure	Gain	IP3	Supply	Power Dissipation
Wu and Hsiao [5]	900 MHz	6 dB	17 dB	-14 dBm	3 V	78 mW
Karanicolas [4]	900 MHz	2.2 dB	15.6 dB	-32 dB	2.7 V	20 mW
Shaeffer and Lee [3]	1.5 GHz	3.5 dB	22 dB	-8 dB	1.5 V	30 mW
Kim et al [6]	1.9 GHz	2.8 dB	15 dB	2 dBm	3.6 V	34 mW
Rafila et al [7] [†]	2.5 GHz	2.5 dB	22 dB	-10 dBm	1.5 V	45 mW
Zhou and Allstot [8]	900 MHz	4.1 dB	12.3 dB	-6 dBm	3 V	18 mW
This work	1.8 GHz	4 dB	10.5 dB	-24 dBm	2.5 V	40 mW

[†] Simulation results.

4. CONCLUSION

A CMOS low-noise amplifier operating at a supply voltage of 2.5 V has been analyzed. Measurement results have shown that the circuit's gain was smaller than predicted by the simulation. This is mainly due to the parasitic resistance of the bondwires that reduce the Q factor of the inductors. Also there is some degradation in performance due to parasitics introduced by the PCB board.

The circuit consumes 40 mW, has a gain of 10.5 dB, and has a noise figure of 4 dB. The main advantage of this circuit is that it can operate at a frequency of 1.8 GHz while maintaining a good linearity. Also, the measurement results are comparable to other CMOS implementations shown in Table 1.

5. ACKNOWLEDGMENTS

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