4-Mb MOSFET-Selected μTrench Phase-Change Memory Experimental Chip

Ferdinando Bedeschi, Roberto Bez, Chiara Boffino, Edoardo Bonizzoni, Egidio Cassiodoro Buda, Giulio Casagrande, *Member, IEEE*, Lucio Costa, Marco Ferraro, Roberto Gastaldi, *Member, IEEE*, Osama Khouri, Federica Ottogalli, Fabio Pellizzer, Agostino Pirovano, Claudio Resta, Guido Torelli, *Senior Member, IEEE*, and Marina Tosi

***Abstract*—A μtrench Phase-Change Memory (PCM) cell with MOSFET selector and its integration in a 4-Mb experimental chip fabricated in 0.18-μm CMOS technology are presented. A cascode bitline biasing scheme allows read and write voltages to be fed to the addressed storage elements with the required accuracy. The high-performance capabilities of PCM cells were experimentally investigated. A read access time of 45 ns was measured together with a write throughput of 5 MB/s, which represents an improved performance as compared to NOR Flash memories. Programmed cell current distributions on the 4-Mb array demonstrate an adequate working window and, together with first endurance measurements, assess the feasibility of PCMs in standard CMOS technology with few additional process modules.**

***Index Terms*—Cascode bitline biasing, nonvolatile memories, Phase-Change Memories, sense amplifier.**

I. Introduction

TODAY, high-performance portable equipment demand nonvolatile memories featuring higher and higher read/write speed and endurance. In recent years, more and more research efforts have been devoted to finding a new technology able to overcome performance and scalability limits of currently dominant Flash memories. Phase-Change Memory (PCM) technology [1]–[4] is one of the most promising candidates for the next generation of nonvolatile memory devices. In fact, PCMs have the capability of improved write throughput versus NOR-based Flash memories and shorter random access time versus NAND-based Flash memories, together with high endurance, fabrication process simplicity, good compatibility with standard CMOS processes, and the potential to be scaled beyond Flash technology limits. A further key advantage is very fine write granularity, as any cell can be independently reprogrammed with no need for block erasing.

Manuscript received November 16, 2004; revised January 25, 2005.

F. Bedeschi, E. C. Buda, G. Casagrande, L. Costa, M. Ferraro, R. Gastaldi, and O. Khouri are with STMicroelectronics, Memory Product Group, 20041 Agrate Brianza, Italy (e-mail: ferdinando.bedeschi@st.com).

R. Bez, F. Ottogalli, F. Pellizzer, A. Pirovano, and M. Tosi are with STMicroelectronics, Central R&D, 20041 Agrate Brianza, Italy.

C. Boffino and E. Bonizzoni are with the Department of Electronics, University of Pavia, 27100 Pavia, Italy. They are also with the Studio di Microelettronica, STMicroelectronics and University of Pavia, 27100 Pavia, Italy.

C. Resta is with the Memory Product Group, STMicroelectronics, 20041 Agrate Brianza, Italy. He is also with the Studio di Microelettronica, STMicroelectronics and University of Pavia, 27100 Pavia, Italy.

G. Torelli is with the Department of Electronics, University of Pavia, 27100 Pavia, Italy.

Digital Object Identifier 10.1109/JSSC.2005.847531

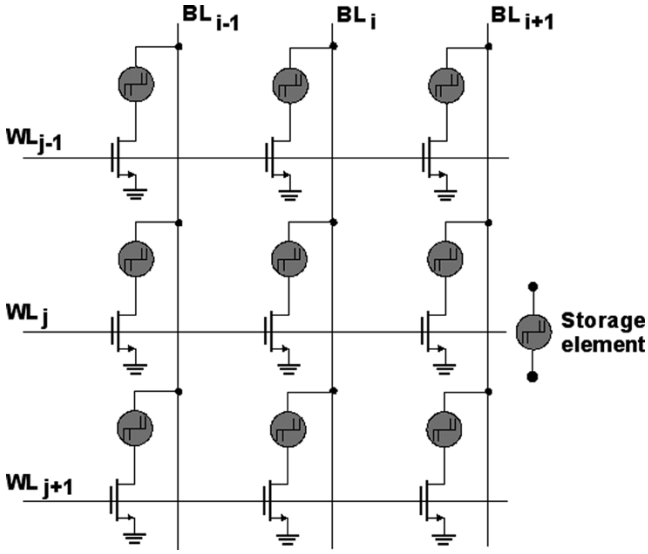


Fig. 1. Detail of the PCM array configuration using an MOS device as a cell selector (WL = wordline; BL = bitline).

This paper presents a 4-Mb PCM experimental chip developed in a 0.18-μm CMOS process to demonstrate the feasibility of a PCM device fabricated by using standard CMOS technology with a limited number of additional process modules. As shown in Fig. 1, the cell selector is implemented by an n-channel MOSFET. Even though a pnp Bipolar Junction Transistor (BJT) can also be employed [4]–[6] to obtain a smaller cell, the use of an MOS device reduces the number of lithographic masks required, thus ensuring lower process cost. This choice also eliminates the problem of cumulative array leakage current due to the reverse-biased base-to-emitter junction of unaddressed BJT selectors. Furthermore, implementing the cell selector with the same (NMOS) device type used in peripheral circuits provides an easier vehicle for PCM technology development and characterization.

The high-performance capabilities of PCM technology were first investigated and assessed on single cells, showing very fast programming together with adequate read margin. The proposed chip was then integrated and experimentally evaluated, thus allowing us to collect multimegabit cell distributions and first statistical endurance data for technology performance assessment.

This paper presents the μtrench PCM cell in Section II. The architecture of the experimental chip is presented in Section III.

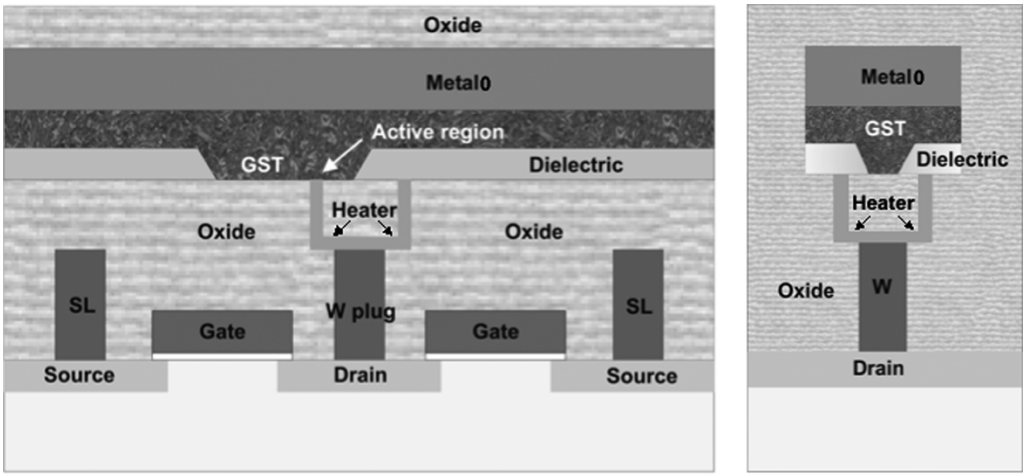


Fig. 2. Schematic cross section of the PCM/MOS array (detail) along (a) the bitline and (b) the wordline directions.

Measurement results are provided in Section IV, and, finally, conclusions are drawn in Section V.

II. Phase-Change Storage Element and Cell Array

In PCMs, also referred to as Ovonic Unified Memories (OUMs), the storage device is made of a thin film of chalcogenide alloy [in our case, $Ge_2Sb_2Te_5$ (GST)]. This material can reversibly change between an amorphous phase (high impedance, RESET state) and a polycrystalline phase (low impedance, SET state) when thermally stimulated, thus allowing information storage. Memory element programming is obtained by properly heating (by means of electrical pulses applied to a suitable heater element) and then cooling a small thermally isolated portion of the chalcogenide material. Once the chalcogenide alloy melts, it completely loses its crystalline structure. When rapidly cooled, the chalcogenide material is locked into its amorphous state (to this end, the cooling operation rate has to be faster than the crystal growth rate). To switch the memory element back to its crystalline state, the chalcogenide material is heated to a temperature between its glass transition temperature and its melting point temperature. This way, nucleation and microcrystal growth occur in tens of nanoseconds, thus leading to a (poly)crystalline state.

From the above, it follows that the storage element can be modeled as a programmable resistor (high resistance = logic 0; low resistance = logic 1). Reading a cell basically consists of measuring the resistance of the addressed storage device. To this end, a predetermined voltage is forced across the storage element of the selected cell, and the resulting current flow is sensed. In practice, the cell current is compared to a trimmable reference current, which, in our experimental chip, can also be driven from an external pad for array characterization purposes.

A schematic cross section of a detail of the cell array along one bitline (which is realized in the lowest metal level, referred to as metal0) and along one wordline is depicted in Fig. 2. To keep the programming current low while still maintaining a compact vertical integration, the definition of the contact area between the heater and the GST element is achieved by the intersection of a thin vertical semimetallic heater and a trench in the heater-to-GST dielectric, referred to as the "μtrench", in which the GST alloy is deposited [7]. The μtrench approach allows defining the PCM active region as the intersection of a sublitho feature and the deposited heater thickness. The cell performance can thus be optimized by tuning the heater-to-GST contact area while still maintaining a good dimensional control. The heating element is connected to the drain region of the MOSFET selector by means of a tungsten plug, while the selector gate, which is split to allow greater driving capability while minimizing cell area, is connected to the metal2 wordline (not shown), which runs orthogonally to the bitlines. The tungsten source line (SL) is connected to a metal1 strap every 64 cells to minimize the overall source line resistance.

TABLE I
Parameters of the Used CMOS Technology

Lithography	0.18 μm
Unit Cell Size	1.55 x 0.85 μm^2
Isolation	Shallow Trench
Gate Oxide	7 nm
Gate Type	Dual-flavour poly & $TiSi_2$
Interconnects	2 Al/Cu

The described μtrench architecture is fully compatible with the use of an MOSFET selector. The PCM cell is integrated by adding its basic process modules (i.e., tungsten precontact, heater, and chalcogenide compound definition) between the front-end and the back-end process blocks. A 0.18-μm CMOS process with 3-V transistors was chosen to integrate the PCM cell in an experimental chip with the goal of proving the performance and the full compatibility of PCM technology with a standard CMOS fabrication process. The basic process architecture (Table I) relies on shallow trench isolation, dual-flavour poly-gate with a gate oxide thickness of 7 nm, and three Al/Cu metallizations (metal0 devoted to bitlines and two interconnect levels, i.e., metal1 and metal2).

Fig. 3 shows a Scanning Electron Microscope (SEM) microphotograph of a detail of the array cross section along one bitline. Although the μtrench architecture is very effective to reduce the programming current and, correspondingly,

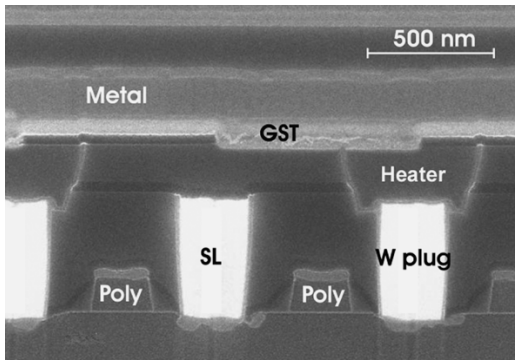


Fig. 3. SEM cross section of the MOS array along the bitline direction.

TABLE II
READ/WRITE CURRENTS AND VOLTAGES FOR SELECTED (SEL) AND UNSELECTED (NO SEL) CELLS

		READ		SET		RESET	
		V(V)	I(μA)	V(V)	I(μA)	V(V)	I(μA)
WL	Sel	1.8	0	3	0	3	0
	No Sel	0	0	0	0	0	0
BL	Sel	0.4	0-80	1.5	300	2.7	600
	No Sel	0	0	0	0	0	0

the MOSFET selector width, the cell size is still quite large ($\sim$ 1.3 μm^2, which corresponds to approximately 40 F^2). As a consequence, this approach is not well suited to high-density stand-alone applications. However, the PCM cell can be easily integrated with a minimum mask overhead (four additional masks in our case) into an advanced CMOS process. This makes the proposed solution well suited to embedded nonvolatile memory applications, as it ensures low cost and reduced process complexity with respect to established nonvolatile memory technologies.

Table II summarizes read/write currents and voltages for selected (Sel) and unselected (No Sel) cells, which are arranged in the memory array as depicted in Fig. 1.

III. CHIP ARCHITECTURE

A schematic block diagram of the experimental chip is illustrated in Fig. 4. The memory is organized in a single 4-Mb array (2048 rows $\times$ 2048 columns). Transistors Y_O (which operate in the saturation region) regulate the bitline voltage to $\sim$400 mV during reading, so as to correctly sense the contents of the selected cell without disturbing its storage element, and to $\sim$1.5 V and $\sim$2.7 V during the SET and the RESET phase, respectively, so as to obtain the required current through the selected cell in both operations (Table II). The regulated read and program voltages are fed to the gates of transistors Y_O by means of the Operation Control (OC) block. In this way, the bitline voltage turns out to be equal to $V_{\mathrm{G,YO}} - (V_{\mathrm{th}} + V_{\mathrm{ov}})$, where $V_{\mathrm{G,YO}}$, V_{th}, and V_{ov} are the gate biasing voltage, the threshold voltage including the body effect contribution, and the overdrive voltage of transistors Y_O, respectively. Natural transistors with a threshold voltage equal to 350 mV were chosen to implement Y_O devices in order to demonstrate that the memory core can be accessed by using voltages not higher than 3.5 V. In read mode, the adopted cascode bitline biasing approach [8] allows fast bitline precharge. It should be pointed out that, during read operations, the bitline voltage has to be adequately low, accurate, and stable in order not to disturb the state of the addressed cell. In this respect, the adopted bitline biasing technique prevents the risk of spurious SET pulses since the cascode structure rejects disturbance injection from the column decoder supply line, referred to as V_A in Fig. 4.

SET and RESET operations require accurate pulses to be applied to the addressed bitlines and, hence, to the selected cells. The pulsed, regulated bitline voltages required in SET and RESET modes are obtained by simply applying suitable voltages to the gates of transistors Y_O. This way, regulated sources are not loaded by any dc current. Transistors M_d discharge all bitlines after any read and write operation (signal *DISCH* high), so as to prevent spurious programming voltages to be applied across unselected cells during next operations.

Programming requires voltages higher than the nominal supply V_{dd} (1.8 V). For this reason, two charge pumps (referred to as X and Y in Fig. 4) were integrated. Charge pump X provides (through regulators) SET, RESET, read, and wordline decoder supply voltages, referred to as V_{SET}, V_{RESET}, V_{READ}, and V_{PCX}, respectively. The other charge pump (Y) is devoted to provide the programming power through the column selector (in this respect, it is worth pointing out that the chosen cascode bitline biasing approach allows the V_A regulator to be designed with relaxed specifications and reduced power consumption). A voltage-tripler scheme [9] was used for both charge pumps. V_A was set to 3.3 V so as to correctly bias the column decoder during both read and program operations.

The OC block provides the appropriate pulsed voltage levels to the gate of natural transistors Y_O. These transistors do not implement a selection level and, hence, one of such devices is associated with each bitline of the array. When a read or a program operation is requested, the gates of all these natural transistors (which are previously discharged so as to completely isolate all memory cells during no-operation) must be raised to the read or the program voltage. Hence, a large load capacitance has to be charged by the corresponding voltage regulators.

In order to ensure fast recovery of the output voltage at the beginning of any read operation, thus minimizing read access time, the topology in Fig. 5 [10] has been used for the read voltage regulator. This regulator consists of an input differential stage A_1, a level shifter A_2, and an NMOS output source follower (MN biased by the resistive network R_1, R_2). The input signal V_{ref} is 0.7 V. The supply voltage V_{CC} (5.2 V) is provided by charge pump X. The chosen regulator structure allows short recovery time together with limited dc power consumption. Indeed, a drop in the regulator output voltage results in an increase of the gate-to-source voltage of transistor MN and, hence, of the output current, thus speeding up output voltage recovery. In addition, the feedback network also increases the gate voltage of the NMOS output device, thus providing a further output current contribution.

The above voltage regulator topology cannot provide adequate swing at internal nodes when output voltages higher than 3 V are required. For this reason, conventional structures [11]

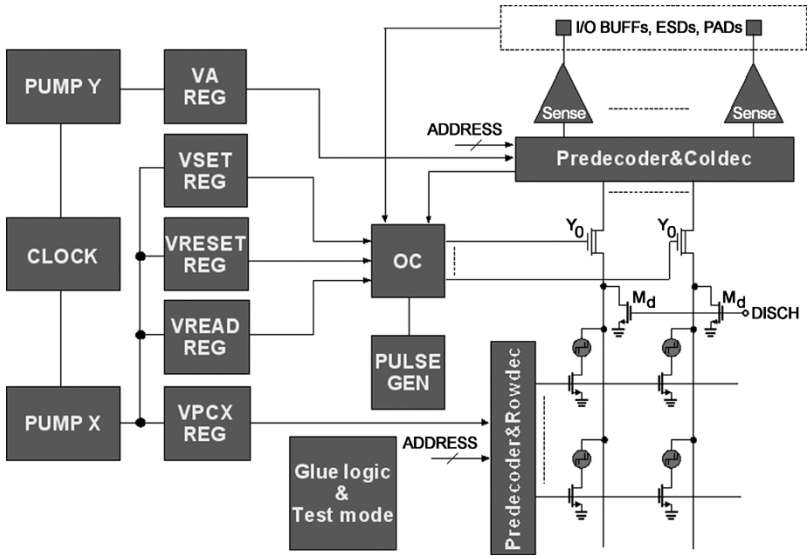


Fig. 4. Block diagram of the experimental chip.

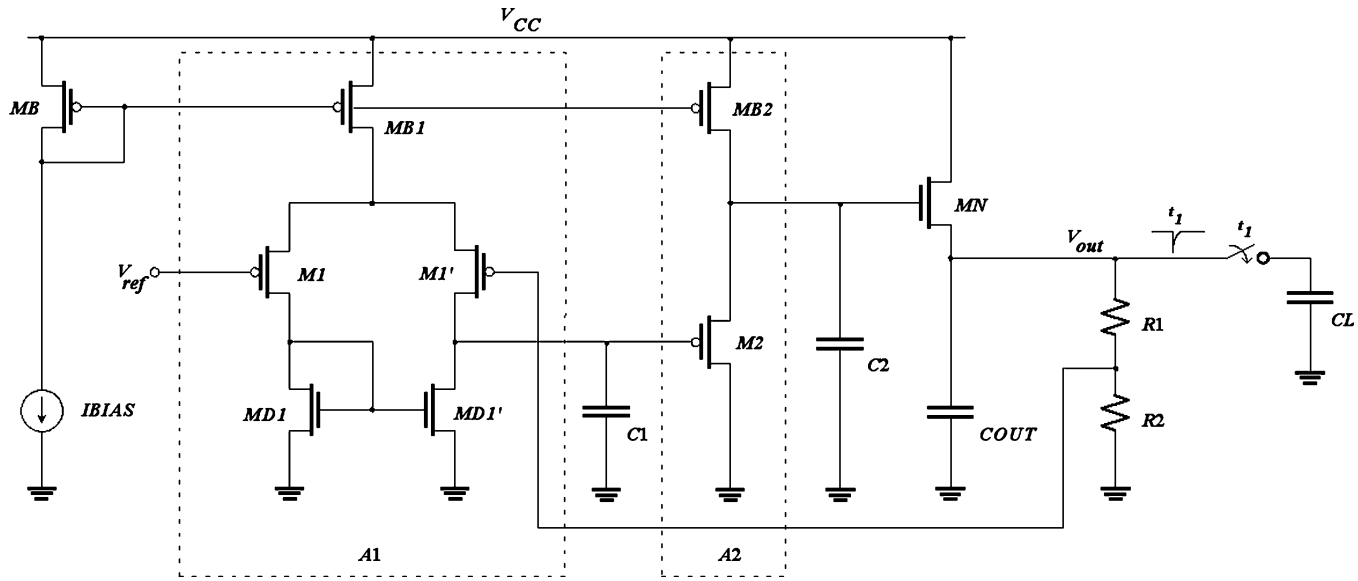


Fig. 5. Circuit diagram of the read voltage regulator (C_L: load capacitance, which is connected to the regulator output at time t_1).

were adopted to regulate $V_{\rm SET}$ and $V_{\rm RESET}$ as well as voltages $V_{\rm PCX}$ and V_A, which have less severe requirements in terms of fast recovery as compared to $V_{\rm READ}$.

A fully symmetrical sense amplifier topology (Fig. 6) [12]–[14] was developed to ensure zero systematic offset together with adequate rejection of disturbances due to capacitive coupling with noisy substrate, power supply, and ground. After bitline precharge and equalization (the corresponding circuitry is not shown in the figure), the current differences $I_M = I_{\rm cell} - I_{\rm ref}$ and $I_R = I_{\rm ref} - I_{\rm cell}$ are obtained (where I_{cell} and $I_{\rm ref}$ are the addressed cell current and the reference current, respectively). The current differences I_M and I_R are integrated onto the parasitic capacitances of nodes *matside* (C_M) and *refside* (C_R). The resulting voltages are compared by means of block A_d, which produces a latched digital output signal *SAOUT*. This signal is then fed to the output buffer and the I/O pad.

IV. Experimental Results

To exploit PCM technology for high-performance applications, short write and read times are mandatory, together with adequate data retention capability. One of the main concerns when speeding up writing operation is the trade-off between fast crystallization and nonvolatility properties of the GST alloy. The GST compound with stoichiometry 2-2-5 was thus employed as a storage material. As previously reported [7], [15], memory elements based on this chalcogenide alloy exhibit fast programming times, 10-year data retention capability at 110 °C, and endurance reaching 10^{11} programming cycles.

Fig. 7 shows the measured programming curves of an MOSFET-selected PCM cell for several SET pulse widths. For very long SET pulses (10 μs), complete crystallization is easily achieved, and a resistance difference of two orders of magnitude between the SET and RESET states is observed. However,

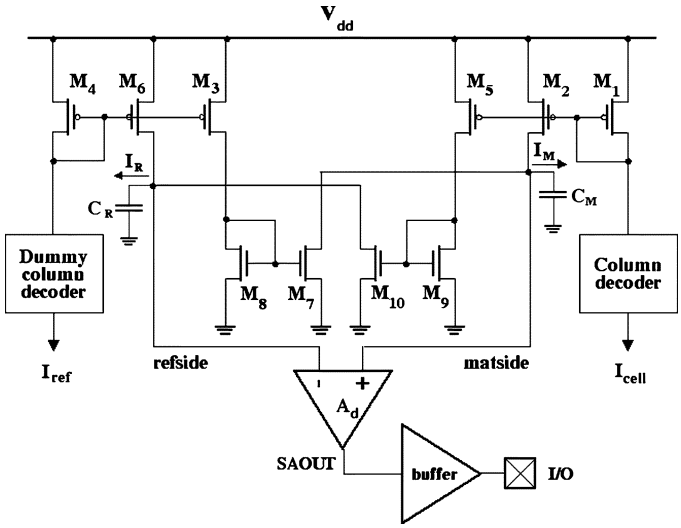


Fig. 6. Circuit diagram of the sense amplifier.

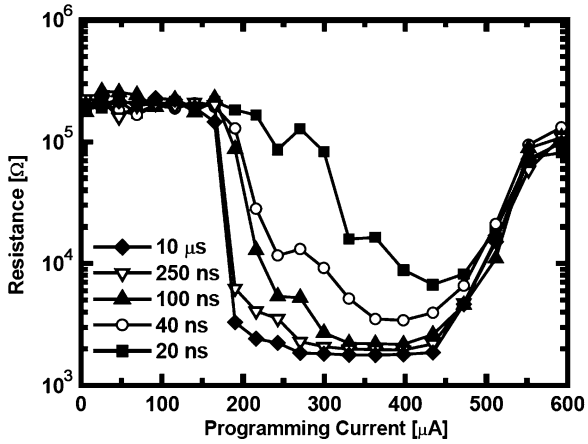


Fig. 7. Programming curves of an MOSFET-selected PCM cell for different SET pulse widths.

this programming time is unacceptable for high-performance products. By reducing the pulse width, the GST alloy is not able to fully crystallize, which results in a higher SET-state resistance. Nevertheless, the characterization performed on single cells (Fig. 7) shows that, for a SET pulse width as low as 20 ns, a factor of 10 in the resistance change between the RESET and SET states is achieved.

A RESET programming current as low as 600 μA (see Table II) is sufficient for our μtrench PCM device. It should be pointed out that this value can be further reduced by suitably tailoring the GST-to-heater contact area and the heater resistance. Since the μtrench width scales with lithography, this will allow a proportional reduction of power consumption in next-generation devices. Optimization of heater material and thickness provides further room for current reduction.

Fig. 8 illustrates the cell resistance in the amorphous state as a function of the RESET pulse width. The three curves correspond to different values of the voltage drops $V_{\mathrm{RESET,DEV}}$ applied across the memory element during RESET. The obtained resistance values range from $10^5\ \Omega$ to $10^6\ \Omega$. When the pulse duration is reduced to 10 ns, a small decrease in the programmed resistance is observed. This effect is ascribed to a delay in reaching

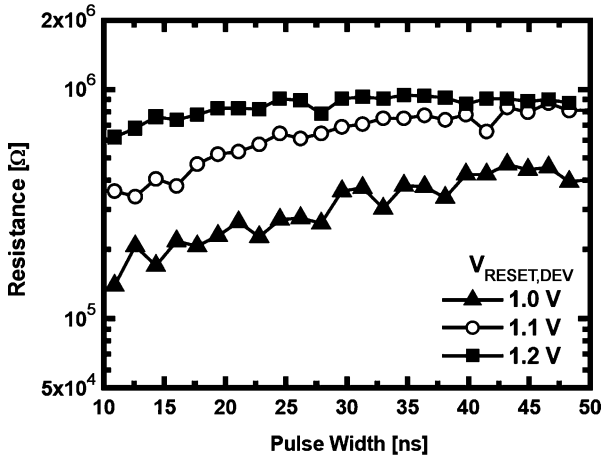


Fig. 8. RESET-state resistance as a function of the programming pulse width for different values of the voltage drop $V_{\mathrm{RESET,DEV}}$ across the storage element.

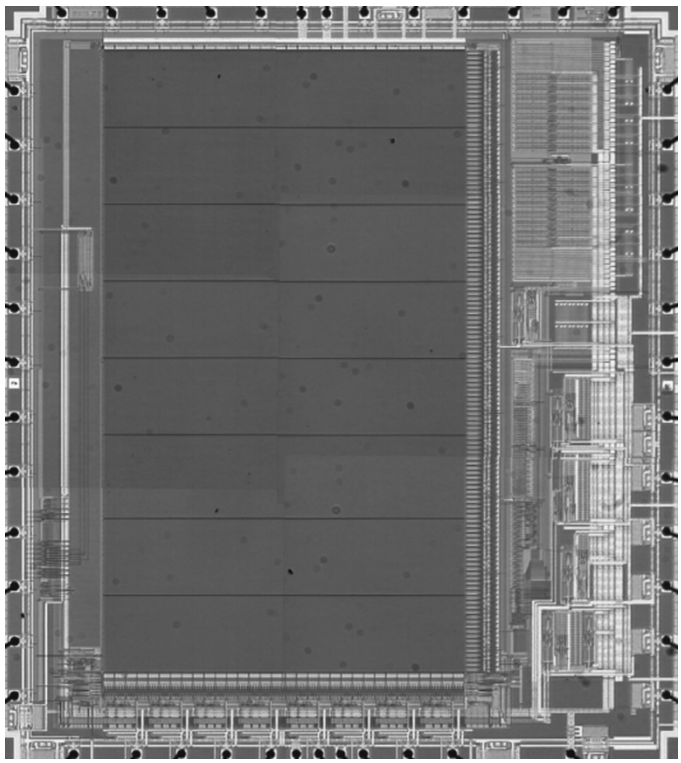


Fig. 9. Microphotograph of the experimental chip.

the thermal steady-state condition in the heated volume, mainly due to the high thermal resistivity of the GST film. Even though a suitable voltage window for read operations has been demonstrated when using SET and RESET pulse widths as small as 20 and 10 ns (Figs. 7 and 8), respectively, consistently larger pulse widths must be chosen to take cell parameter distribution and reliability into account.

Fig. 9 shows a chip microphotograph of the 4-Mb experimental chip. Fig. 10 illustrates the measured voltage waveforms when reading a SET cell (WL = wordline; BL = bitline; CE_N = chip enable, active low; $OUTPUT\ DATA$ = I/O pin; V_{dd} = 1.8 V). The read access time is 45 ns.

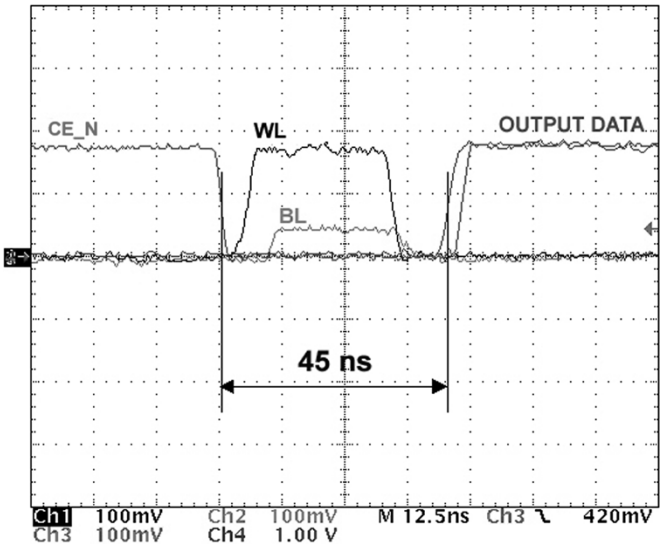


Fig. 10. Measured voltage waveforms when reading a SET cell (CE_N, WL, and BL: active probes, attenuation by a factor of 10).

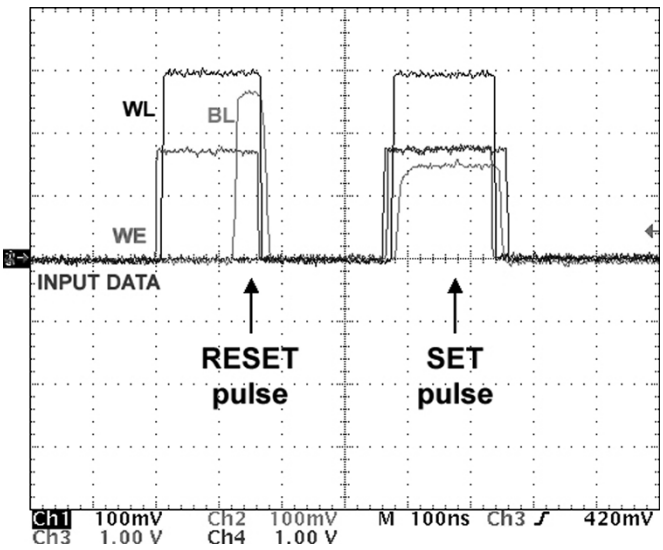


Fig. 11. Measured voltage waveforms during SET and RESET operations (WL, BL: active probes, attenuation by a factor of 10).

Fig. 11 shows the measured voltage waveforms in consecutive RESET and SET operations (WE = write enable, active high; $INPUT\ DATA$ = I/O pin; $V_{\rm dd} = 1.8$ V). During the RESET operation, the falling edge of the addressed wordline voltage has to be very sharp so as to allow the melted GST material to be rapidly cooled, thus correctly amorphizing the cell. This operation, referred to as quenching, is carried out by keeping the wordline fall time within a few nanoseconds (in our case, 2 ns). For the measurement in Fig. 11, a relaxed RESET pulse of 40 ns and a SET pulse of 150 ns were employed in order to obtain adequately narrow cell distributions. In the proposed experimental chip, a write parallelism of 8 was implemented. The write throughput, which is determined by the 200-ns SET time (SET pulse duration +50 ns due to circuitry delay), is therefore 5 MB/s. The achieved write throughput represents a strong improvement with respect to NOR Flash memory performance. A write throughput of 10 MB/s can be easily achieved

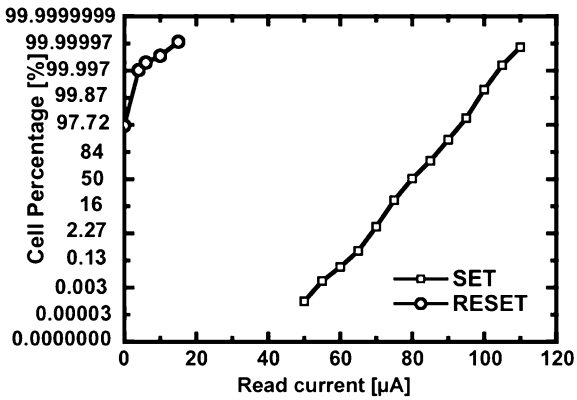


Fig. 12. Read currents distributions of a 4-Mb array after SET and RESET operations.

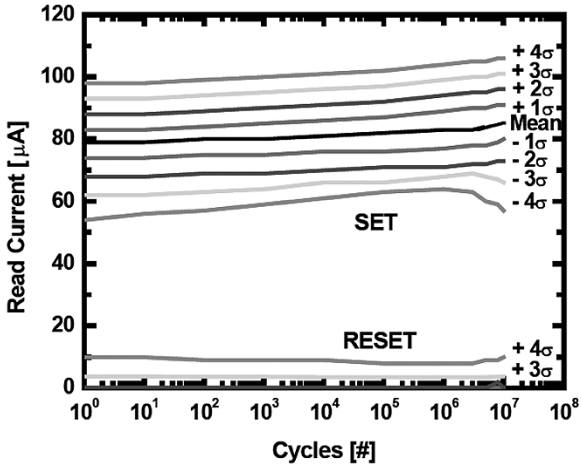


Fig. 13. Preliminary endurance measurements.

by increasing the write parallelism to 16, still with an acceptable current drawn from power supply $V_{\rm dd}$ (30 mA, also taking the efficiency of the charge pumps into account).

Several measurements were also successfully performed to assess the whole chip functionality. Fig. 12 illustrates the cell current distributions of the 4-Mb array after SET (150-ns pulses) and RESET (40-ns pulses) operations. The achieved current window is more than adequate for robust reading operation.

Preliminary results of endurance tests are illustrated in Fig. 13. This figure shows the SET/RESET current window evolution of the population of 10 samples, as a function of the number of SET/RESET cycles. The figure shows both the mean value and the values corresponding to a deviation of $\pm\sigma$, $\pm 2\sigma$, $\pm 3\sigma$, and $\pm 4\sigma$ in the obtained read current distributions (the mean value of the RESET-state read current is too low to be appreciated in the figure). These preliminary results demonstrate excellent endurance performance of PCM technology.

V. Conclusion

A 4-Mb PCM experimental chip using an MOS device as a cell selector, integrated with 0.18-μm CMOS technology, has been presented. The high-performance capabilities of μtrench PCM cells have been experimentally evaluated. A read access time of 45 ns and a write throughput of 5 MB/s were measured,

thus demonstrating improved performance as compared to currently dominant NOR Flash memories. SET and RESET cell characterization data, read current distributions and first statistical measurements have been presented, assessing the feasibility of PCM technology in standard CMOS fabrication process.

REFERENCES

[1] S. Tyson, G. Wicker, T. Lowrey, S. Hudgens, and K. Hunt, "Nonvolatile, high density, high performance phase-change memory," in *Proc. 2000 IEEE Aerospace Conf.*, vol. 5, Mar. 2000, pp. 385–390.

[2] J. Maimon, E. Spall, R. Quinn, and S. Schnur, "Chalcogenide-based nonvolatile memory technology," in *Proc. IEEE Aerospace Conf.*, vol. 5, Mar. 2001, pp. 2289–2294.

[3] S. Lai and T. Lowrey, "OUM—A 180 nm nonvolatile memory cell element technology for stand-alone and embedded applications," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2001, pp. 803–806.

[4] M. Gill, T. Lowrey, and J. Park, "Ovonic unified memory—A high performance nonvolatile memory technology for stand-alone memory and embedded applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.*, vol. 1, Feb. 2002, pp. 458–459.

[5] W. Y. Cho, B.-H. Cho, B.-G. Choi, H.-R. Oh, S.-B. Kang, K.-S. Kim, K.-H. Kim, D.-E. Kim, C.-K. Kwak, H.-G. Byun, Y.-N. Hwang, S.-J. Ahn, G.-T. Jung, H.-S. Jung, and K. Kim, "A 0.18 μm 3.0 V 64 Mb nonvolatile phase-transition random-access memory (PRAM)," in *IEEE Solid-State Circuits Conf. Dig. Tech. Pap.*, vol. 1, Feb. 2004, pp. 40–41.

[6] F. Bedeschi, C. Resta, O. Khouri, E. Buda, L. Costa, M. Ferraro, F. Pellizzer, F. Ottogalli, A. Pirovano, M. Tosi, R. Bez, R. Gastaldi, and G. Casagrande, "An 8 Mb demonstrator for high-density 1.8 V phase-change memories," in *Proc. Symp. VLSI Circuits*, Jun. 2004, pp. 442–445.

[7] F. Pellizzer, A. Pirovano, F. Ottogalli, M. Magistretti, M. Scaravaggi, P. Zuliani, M. Tosi, A. Benvenuti, P. Besana, S. Cadeo, T. Marangon, R. Piva, A. Spandre, R. Zonca, A. Modelli, E. Varesi, T. Lowrey, A. Lacaita, G. Casagrande, P. Cappelletti, and R. Bez, "Novel μtrench phase-change memory cell for embedded and stand-alone nonvolatile memory applications," in *Proc. Symp. VLSI Technology*, Jun. 2004, pp. 18–19.

[8] F. Bedeschi, C. Boffino, E. Bonizzoni, O. Khouri, C. Resta, and G. Torelli, "Bit-line biasing technique for phase-change memories," in *Proc. Int. Conf. Signal and Electronic Systems*, Sep. 2004, pp. 229–232.

[9] M. Zhang, N. Llaser, and F. Devos, "Improved voltage tripler structure with symmetrical stacking charge pump," *Electron. Lett.*, vol. 37, pp. 668–669, May 2001.

[10] F. Bedeschi, C. Boffino, E. Bonizzoni, O. Khouri, C. Resta, and G. Torelli, "Fast-recovery CMOS voltage regulator for large capacitive loads," in *Proc. Int. Conf. Signal and Electronic Systems*, Sep. 2004, pp. 349–352.

[11] G. A. Rincón-Mora and P. E. Allen, "Low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[12] M. Pagliato, P. Rolandi, and M. Montanaro, "Reading circuit and method for a multilevel nonvolatile memory," U.S. Patent 6,657,895, Dec. 2, 2003.

[13] F. Bedeschi, E. Bonizzoni, O. Khouri, C. Resta, and G. Torelli, "A fully symmetrical sense amplifier for nonvolatile memories," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, May 2004, pp. 625–628.

[14] E. Confalonieri, "Sense amplifier structure for multilevel nonvolatile memory devices and corresponding reading method," U.S. Patent 6,822,906, Nov. 23, 2004.

[15] F. Ottogalli, A. Pirovano, F. Pellizzer, M. Tosi, P. Zuliani, P. Bonetalli, and R. Bez, "Phase-change memory technology for embedded applications," in *Proc. Eur. Solid-State Device Research Conf.*, Sep. 2004, pp. 293–296.

Roberto Bez was born in Milan, Italy, in 1961. He received the Doctor degree in physics from the University of Milan in 1985.

In 1987, he joined the Central R&D Department of STMicroelectronics and started to work on Non-Volatile Memory (NVM) technologies. In the 1990s, he participated in the development of the NOR Flash memory technology, in the first phase as expert of the device physics and reliability and in the second phase as project leader of the multilevel product development. In 2000, he started to investigate new NVM technologies, alternative to the floating-gate-based Flash. Since 2001, he has been working on the development of Phase-Change Memory technology. Currently, he is the high density and emerging memories Director in the NVM Technology Development of the Front-end Technology and Manufacturing group. He has authored many papers, conference contributions, and patents on topics related to NVM. He has been a Lecturer in electron device physics at the University of Milan and in nonvolatile memory devices at the University of Padova, Polytechnic of Milan, and University of Udine.

Chiara Boffino was born in Pavia, Italy, on November 7, 1977. She received the Dr.Eng. degree (*summa cum laude*) in electronics from the University of Pavia, Pavia, Italy, in 2002. She is currently working toward the Ph.D. degree in electronic, computer, and electrical engineering in the Department of Electronics at the same university.

Since 2002, she has been holding a grant from STMicroelectronics within the "Studio di Microelettronica," Pavia, in the Memory Product Group. Her current research interests include CMOS analog circuit design with particular focus on applications for phase-change memories.

Edoardo Bonizzoni was born in Pavia, Italy, in 1977. He received the Dr.Eng. degree (*summa cum laude*) in electronics from the University of Pavia in 2002, where he is currently working toward the Ph.D. degree in electronic, computer, and electrical engineering.

Since 2002 he has been holding a grant from STMicroelectronics, within the "Studio di Microelettronica," Pavia. His research is in the areas of analog circuit design, VLSI, and nonconventional nonvolatile memories with particular regard to phase-change memories.

Ferdinando Bedeschi was born in Taranto, Italy, in 1973. He received the Dr.Eng. degree (*summa cum laude*) in electronics from the University of Pisa, Pisa, Italy, in 1998.

Since 1999, he has been with STMicroelectronics, Agrate Brianza, Italy, where he currently is project leader of the Memory Product Group. His activity is focused on test-vehicle designs for emerging technologies development.

Egidio Cassiodoro Buda was born in Lentini, Italy, in 1970. He received the Laurea degree in electronics from the University of Catania, Catania, Italy, in 2001. His thesis concerned the field of ferroelectric memories (FRAM) focused on ferroelectric capacitor characterization.

In the same year, he joined the MPG-R&D testing Group, STMicroelectronics, Catania, Italy. His testing activity started in the area of Page-Flash memories, finalized to the process development for smart-card applications. Since 2003, his testing activity has been focused on phase-change memory process development.

Giulio Casagrande (M'99) was born in Trento, Italy, in 1951. He received a degree in electronic engineering from the University of Padova, Padova, Italy, in 1977.

In 1977, he joined ST Microelectronics, Milan, Italy, where he first worked on the design of EPROMs and EEPROMs, and then he led the design and engineering team that developed the first generations of Flash Memories in ST. He has covered different managerial roles in nonvolatile memory development and engineering, including the creation and the direction of the Catania Development Center for the Memory Products Group. He is now Director of R&D for the Memory Products Group, focusing on advanced Flash design solutions also for embedded applications, assessment and development of disruptive emerging memories, computer-aided design, and design methodology. He has authored papers and Short Courses at IEEE conferences and holds several patents in the nonvolatile memory field.

Lucio Costa was born in Messina, Italy, on July 13, 1972. He received the Laurea degree in electronics from the University of Messina, Messina, Italy.

In May 2002, he joined STMicroelectronics, Catania, Italy. In September of the same year, he joined the Memory Product Group, STMicroelectronics, Agrate Brianza, Italy, where his testing activity is focused on phase-change memory process development.

Marco Ferraro was born on May 29, 1976 in Tricase, Italy. He received the "Laurea" degree in telecommunication engineering from the University of Pisa, Pisa,Italy, in 2001. His thesis discussed a proposal of a measurement based admission control for DiffServ IP networks.

From January to May 2002, he was with the TeLeCommunications NETwork GRouP (TLCNETGRP), Department of Information Engineering, University of Pisa, working on development of IP network models with OPNET simulator. Since June 2002, he has been a Product Engineer with ST Microelectronics, Agrate Brianza, Italy.

Roberto Gastaldi (M'77) graduated in electronic engineering from the Polytechnic Institute of Milan, Milan, Italy, in 1977.

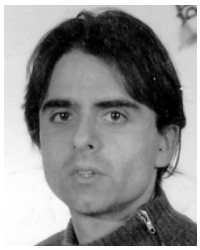
In the same year, he joined ST Microelectronics, Milan, as a Researcher involved in the characterization and modeling of electrical conduction in thin oxides. In 1982, he moved to the Memory Design Department as a Designer, where he was involved in EPROMs and the first generations of Flash products. He was a Design Manager of the EPROM Division and later a Design Director of the Ram&Automotive Flash Division, leading design activities in the area of SRAM/PSRAM and NOR Flash products. Presently he serves as the Design Director of R&D of the Memory Product Group, ST Microelectronics, Agrate Brianza, Italy, where he is involved with emerging memories architecture and design.

Osama Khouri was born in Jerusalem, Palestine, on November 2, 1961. He received the "Laurea" degree in electronic engineering from the University of Pavia, Pavia, Italy, in 1988, the M.S. degree in economics and management from the International High School "Enrico Mattei," San Donato Milanese, Italy, in 1991, and the Ph.D. degree in electronic and computer engineering from the University of Pavia in 2000.

From 1988 until 1990, he was with Olivetti Computers in Jordan. During his doctoral work, he worked in collaboration with STMicroelectronics under a grant. In January 2000, he joined the Memory Product Group at "Studio di Microelettronica," STMicroelectronics, Pavia, as a Design Engineer, where he was involved with 64-Mb multilevel Flash memory, focusing his activity on design and development of high-voltage management system including high-performance analog ciruits and very fast voltage regulators; after that he worked on a 0.13-μm Flash memory test-chips where he designed and developed advanced architectural and circuital solutions for the storage of 4 b/cell. He worked on the design and the development of nonvolatile memories based on phase-change materials where he designed 4-Mb and 8-Mb phase-change memory test-chips. Currently, he is with the NAND Flash Division as a Project Leader of a 2-Gb NAND Flash memory device. He is the author/coauthor of more than 30 patents and 18 publications.

Federica Ottogalli was born in Mestre, Italy, in 1973. She received the Laurea degree in physics from the University of Padova, Padova, Italy, in 1998. Her thesis focused on crystallographic characterization by RBS channeling and modeling of III–V compounds (GaN-based) epitaxially grown on Al_2O_3.

She joined the Non-Volatile Memory Technology Development Group, Central R&D Division, STMicroelectronics, Agrate Brianza, Italy, in 1999, where she was involved with the process integration of Flash memories (for the 0.18- and 0.16-μm node technologies) and of phase-change nonvolatile memory cells based on chalcogenide materials. Her current activity, since 2002, is focused mainly on electrical characterization of phase-change memory cells.



Fabio Pellizzer was born in 1971. He received the B.S. degree in electronic engineering in 1996 from the University of Padova, Italy, with a thesis on characterization and reliability of thin gate oxides in MOS transistors.

He joined STMicroelectronics, Agrate, Italy, in 1998. His research focused on thin dielectrics characterization and modeling. On this subject, he has written several technical papers for international journals and conferences. In 2001, he started working on the electrical characterization of nonvolatile memories based on chalcogenide materials and participating in the process architecture definition. He has authored or coauthored many papers, conference contributions, and patents on topics related to phase-change memories.

Agostino Pirovano was born in Italy in 1973. He received the Laurea degree in electrical engineering from the Politecnico di Milano, Italy, in 1997, and the Ph.D. degree from the Department of Electrical Engineering, Politecnico di Milano, Italy, in 2000.

He joined the Dipartimento di Elettronica e Informazione, Politecnico di Milano, in 2000, working in the silicon device and technology area. His research interests include the modeling and characterization of transport properties and quantum effects in MOS devices and the physics of Si/SiO interface. In 2001 and 2002, he was a consultant for STMicroelectronics working on the development of chalcogenide-based phase-change memories. Since 2002, he has taught optoelectronics at the Politecnico di Milano, where he has been a Lecturer since 1999. He is with the Non-Volatile Memory Process Development Group of the Central Research and Development of STMicroelectronics, working on the electrical characterization and modeling of phase-change nonvolatile memory cells.

Claudio Resta was born in Tirano, Italy, in 1972. He received the Laurea degree in electronic engineering from the University of Pavia, Pavia, Italy, in 2000. His thesis presented an interface circuit for electromagnetic sensors in CMOS technology.

Since 2001, he has been with the Memory Product Group—R&D of STMicroelectronics, Agrate Brianza, Italy. His activity is focused on test-vehicle design for emerging technologies, development, and characterization of phase-change memories.

Guido Torelli (M'90–SM'96) was born in Rome, Italy, in 1949. He received the Laurea degree (with honors) in electronic engineering from the University of Pavia, Pavia, Italy, in 1973.

After graduating, he spent one year with the Institute of Electronics, University of Pavia, on a scholarship. In 1974, he joined SGS-ATES (now part of STMicroelectronics), Agrate Brianza, Italy, where he served as a Design Engineer for MOS ICs, where he was involved in both digital and analog circuit development, and where he became Head of the MOS ICs Design Group for Consumer Applications. Since 1987, he has been with the Department of Electronics, University of Pavia. His research interests are in the area of MOS integrated circuit design. Currently, his work focuses mainly on the fields of nonvolatile memories and CMOS analog and mixed analog/digital circuits.

Prof. Torelli was a corecipient of the Institute of Electrical Engineers Ambrose Fleming Premium (session 1994–1995). He is a member of the Italian Association of Electrical and Electronics Engineers (AEI).

Marina Tosi was born in Verona, Italy, in 1955. She received the Laurea degree in physics from the University of Padova, Italy, in 1978.

She joined STMicroelectronics in 1979 working in the Central R&D group on MOS transistors. Since 1987, she has been working in memories, EPROM, and FLASH, with particular interest in reliability. Since 2001, she has been working with the Non-Volatile Memory Process Development Group on the process architecture and electrical characterization of phase-change nonvolatile memory cells.